

Design of the TangerineSDR Clock Module

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TangerineSDR Clock Requirements

- 122.88 MHz clock to drive RF modules
- Pulse-per-second and timestamps for data tagging
- 10 MHz general purpose reference signal
- Total Electron Count observation/reporting
- Specifications (as declared by the team):
 - Frequency accuracy (long-term): <1x10⁻¹²
 - Frequency stability: $<1x10^{-9}$ (1 part per billion) at tau >= 1 second
 - PPS accuracy: within 100 nanoseconds of UTC(USNO)
 - PPS jitter: <10 nanoseconds
 - Phase noise (122.88 MHz):
 - -80 dBc/Hz @ 100 Hz offset
 - -150dBc/Hz @ 100 kHz offset



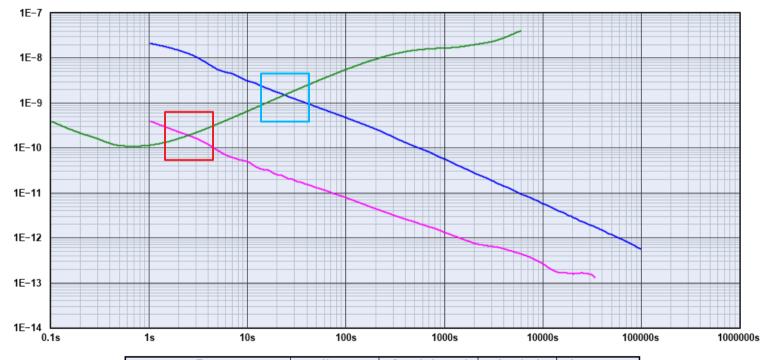
GPSDO Concepts

- GPS has long-term accuracy and stability, but short term noise
- Crystal oscillator has short-term stability but drifts and is environmentally sensitive.
- Use phase-lock loop with suitable time constant to steer crystal to stay lined up with GPS
- Goal is to match rising ADEV of XO with falling ADEV of GPS as measurement period ("tau") increases



The Magic Plot

Allan Deviation $\sigma_y(\tau)$



Trace	Notes	Sample Interval	Acquired	Instrument
Sparkfun EM-406A (SiRF III)	TVB Maser	1 s	400000 pts	HP 53132A
ZED-F9T Corrected PPS	vs HP 5071A	1 s	140000 pts	TICC
Vectron 125 MHz TCXO	vs HP 5071A	0.100 s	246082 pts	TICC

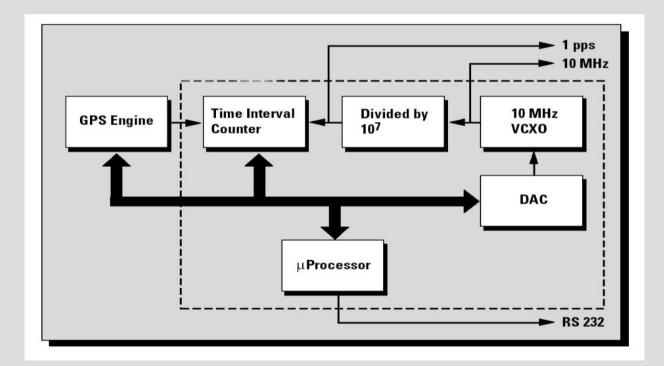


GPSDO Concepts

- Traditional implementation:
 - GPS with pulse-per-second ("PPS") output
 - 10 MHz TCXO/OCXO divided down to PPS
 - Compare phase of PPS and steer oscillator to follow GPS
 - PLL time constant typically 100 to 1000 seconds
 - Tune loop to ADEV crossover point
 - Added features:
 - "Holdover" to keep reasonable frequency if GPS signal lost
 - MCU "learns" aging and tempco of oscillator to improve holdover
 - Variable loop bandwidth for faster acquisition



Traditional GPSDO Architecture



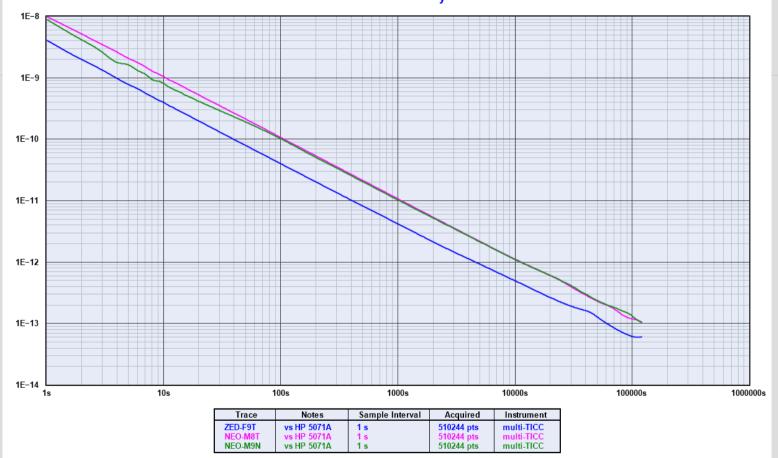


Do Newer GPS Modules Offer Advantages?

- Traditional GPS PPS have jitter of ~10–50 nanoseconds
 - That establishes the ADEV starting point
 - Lower jitter means shorter PLL time constant, means maybe cheaper oscillator will do
- Newer GPS modules offer:
 - Higher internal clock frequency to lower jitter
 - "Sawtooth" error correction
 - Dual-Frequency operation (ZED-F9 modules)

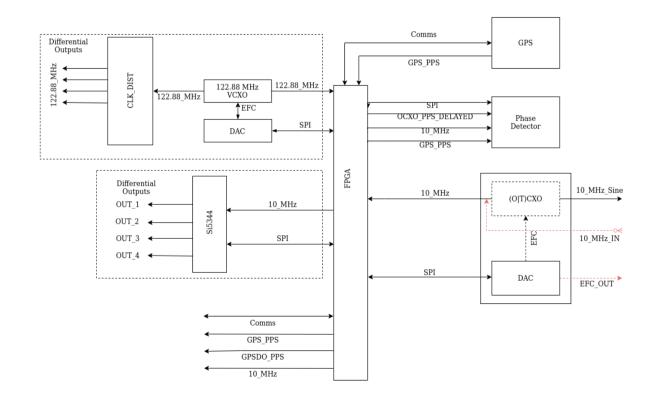


Allan Deviation $\sigma_y(\tau)$





Clock Module Mark I



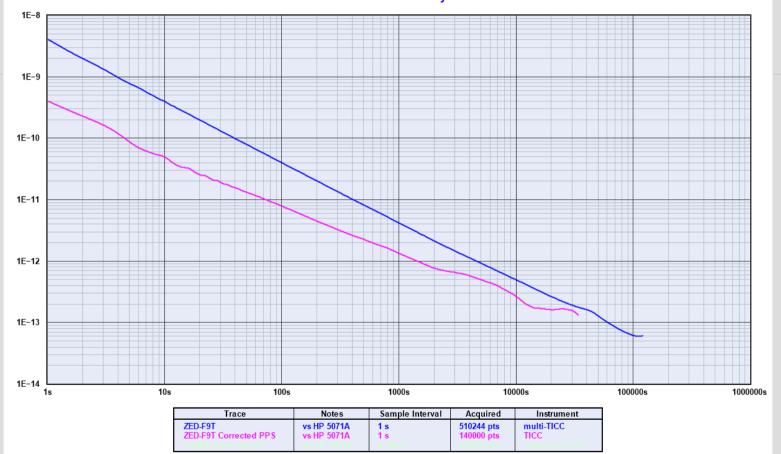


Allan Deviation $\sigma_y(\tau)$



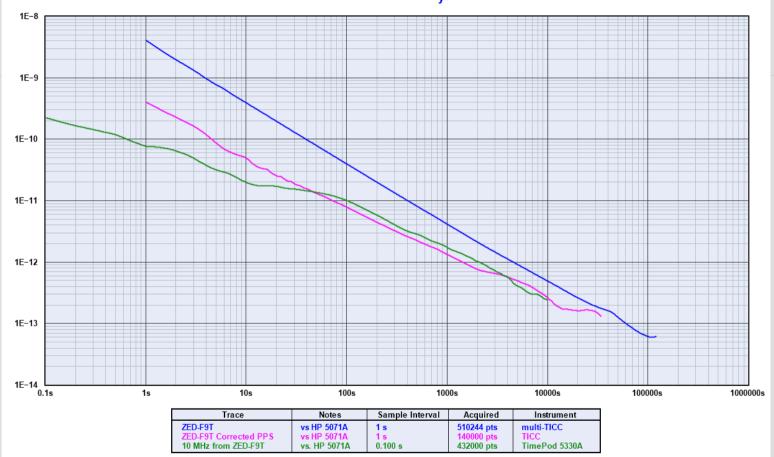


Allan Deviation $\sigma_V(\tau)$





Allan Deviation $\sigma_y(\tau)$





REF 10.0 dBm

SPAN

RES BW 10 Hz

hρ 10 dB/

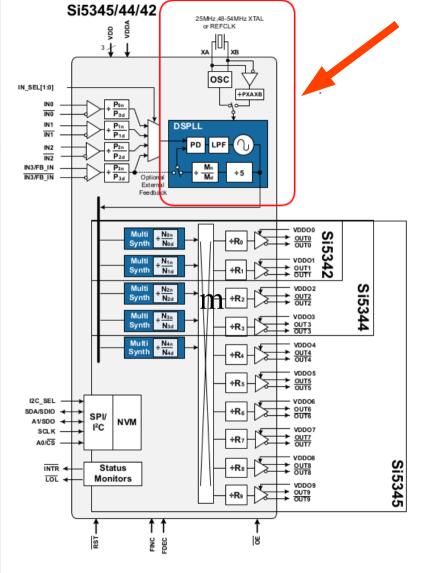
Phase Noise *L*(f) in dBc/Hz -50.0-60.0 -70.0 mmmmm -80.0 A -90.0 -100.0 ATTEN 20 dB + 20 dB 1,000 kHz 10 Hz 100 Hz 1 kHz 10 kHz 100 kHz Sample Interval Trace Notes Acquired Instrument ZED-F9T 10 MHz vs. ULN 0.001 s 300000 pts TimePod 5330A A TANK CENTER 10,000000 MHz SPAN 1,000 kHz

VBW 10 Hz SWP 20 sec



The Si5344 "Jitter Attenuator" Chip

- Intended for on-board cleanup of distributed clock signals
- Locks internal low-noise reference to external clock input
 - Dirty input, clean output!
- 4 independent outputs at any freq from 100 Hz to 1028 MHz
- 4 inputs from 8 kHz to 750 MHz
- Programmable PLL bandwidth
- Modest holdover capability
- Fail-over between inputs





Phase Noise

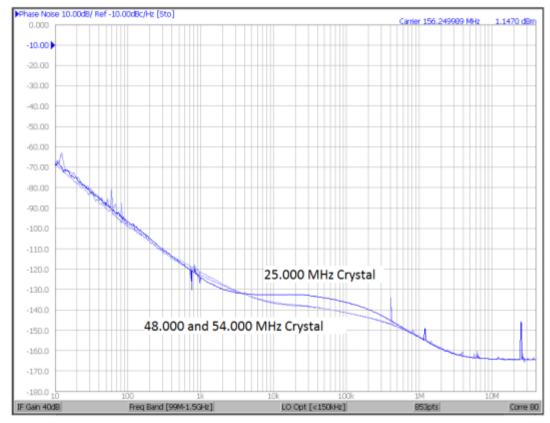
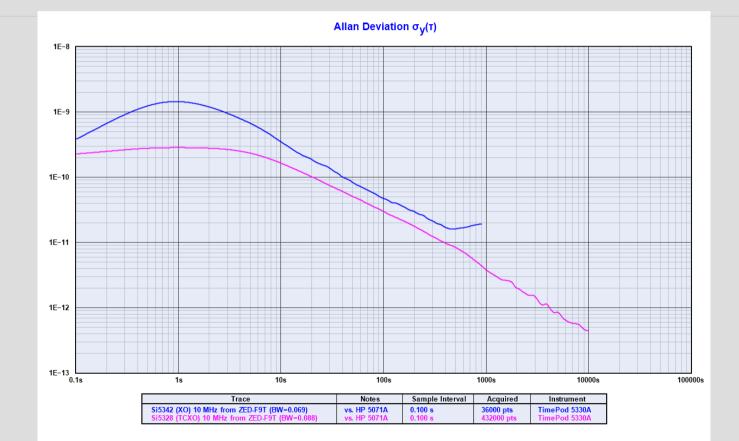


Figure 2. Si5345 156.250 MHz Phase Noise Comparison Using 25.000, 48.000, and 54.000 MHz Crystals as the XA/XB Reference

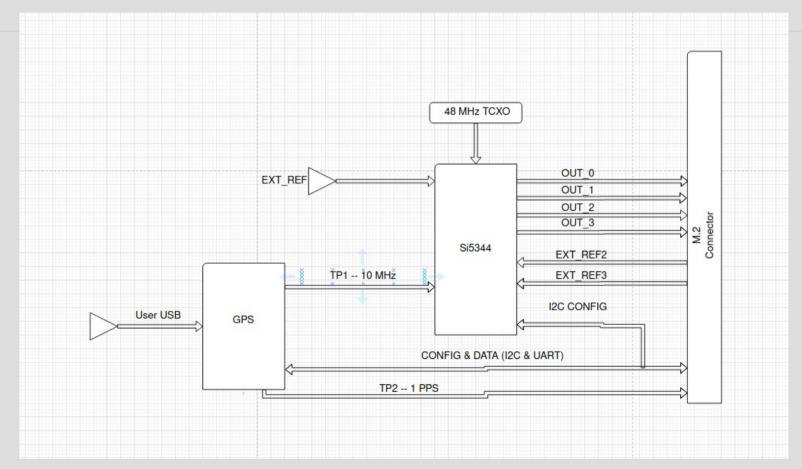


Short-Term Stability





Clock Module Mark 2





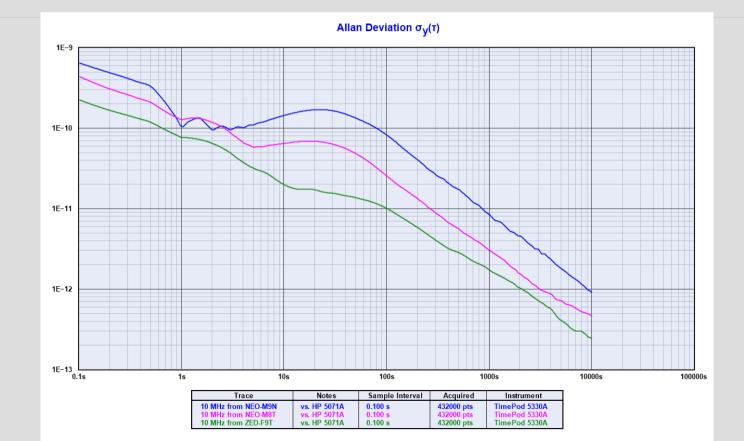
Performance Levels

- Base No GPS, requires external frequency reference
- Bronze NEO-M9N; modest RF; no PPS (\$14.15*)
- Silver NEO-M8T; better RF; has PPS (\$51.85*)
- Gold ZED-F9T; best RF; has PPS; TEC (\$154.33*)

* u-blox qty. 100 price as of 23 Nov. 2020 for GPS module only

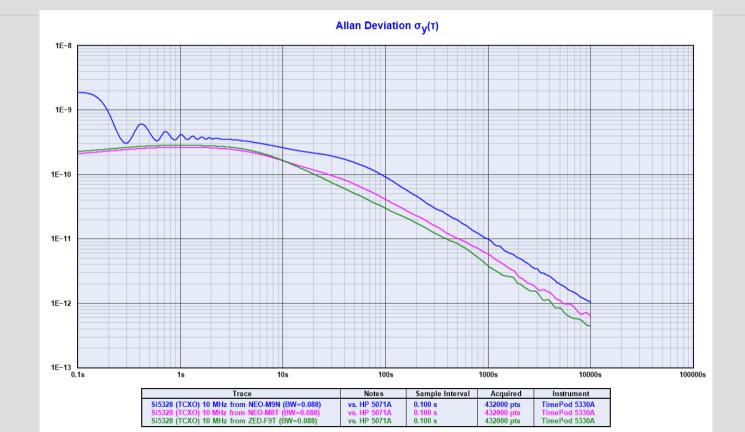


GPS Raw 10 MHz Performance



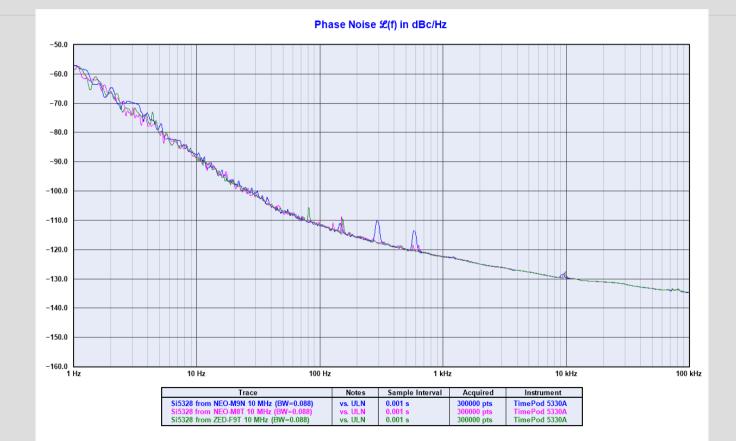


Si5328 Narrow Bandwidth Performance



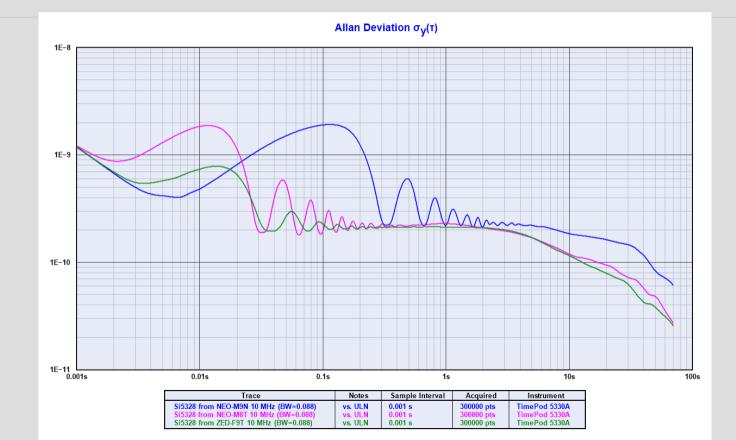


Si5328 Narrow Bandwidth Phase Noise



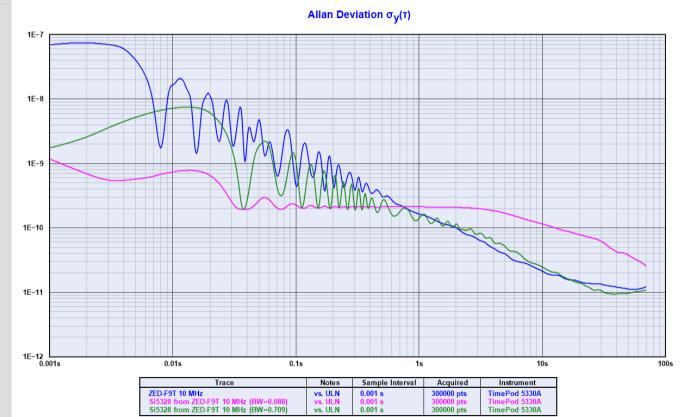


Si5328 Narrow Bandwidth Fast ADEV





Si5328 Bandwidth Impact on ADEV



Si5328 Bandwidth Impact on Phase Noise





Breadboard Performance

• Switch to TimeLab...