TangerineSDR

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RF Receiver Module (RXM-5001D)

Requirements Document

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VERSION HISTORY

Version Number	Implemented By	Revision Date	Approved By	Approval Date	Description of Change
0.1	T. McDermott	7/17/2019			Original Issue
0.1.1	T. McDermott	August 1, 2019			Reformat and Change Document Name
0.2	T McDermott	August 6, 2019			Change document to apply only to RXM-5001D variant. Change document number and name.
0.2.1	T. McDermott	August 9, 2019			Clean up errors from document conversion in V0.2

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1. Introduction

1.1. Scope

This document applies only to the RXM-5001D Receiver Variant. This module uses two 14-bit AD converters, and is intended to support the Personal Space Weather Station (PSWS). It contains requirements in support of PSWS that may or may not exist for other receiver module variants.

1.2. Purpose

The Tangerine SDR Receiver Module RXM-5001D is a dual-channel module that contains two complete receivers, from the antenna connector through the ADC. It receives two radio frequency signals in the 100 kHz to 30 MHz range, optionally filters and attenuates the signals, digitizes the signals with a low-jitter clock, and transfers the digitized samples to the Tangerine SDR Data Engine module.

The unit provides an integrated noise source that can programmatically connect each receiver to a broadband noise source of known amplitude in order to calibrate the receiver sensitivity. The unit may use a single noise source for the two receiver channels, but it will require two relays (one per channel) to select the noise source. It will also contain two plug in RF filters, two programmable attenuators, etc. The noise signal is injected ahead of the attenuator and filter. This provides the ability to capture test data that will allow determination of filter and other characteristics being applied to the received RF signal.

1.3. Cost Goals

The cost goal of the RXM-5001D Dual Channel RF module is $TBD.

1.4. References

- The RF module detailed form factor, mechanical layout, electrical signal interconnection, connectors and pinouts, and electrical specifications are described in the Interface Control Document (ICD) for the RXM-5001D module.
- Tangerine SDR Clock Module Specification. Sets the jitter, frequency accuracy, channel-to-channel coherence and phase noise of the clock inputs to the RF Module.
- Data Engine ICD.
- Dual channel ADC, and ADC driver integrated circuit manufacturer data sheets.

1.5. Form Factor Objective

The form factor will be defined in the ICD document for the RF Modules.

Discussion (for further study):

The module is planned to fit in the RFM single module size identified in the drawing, and is >45mm wide by TBD mm in length. An MEC connector is on one 45+ mm side and two SMA connectors on the opposite 45+ mm side.

The anticipated module density is very tight for the dual-channel unit. Another option may be to use a dual module of dimensions roughly 85 mm by TBD mm. This would eliminate the ability to equip the second RFM slot with a transmitter module, but a transmitter module may not be needed in the PSWS application.

2. Power Supply

The RF Module shall be powered from:

- +1.8 VDC, and shall draw less than TBD mA.
- +3.3 VDC, and shall draw less than TBD mA.
- +5VDC, and shall draw less than TBD mA.
- TBD: -5 VDC, and shall draw less than TBD mA. The ADC driver IC may require -5 VDC. If the ADC driver can be designed to operate only from +5 VDC, then this supply could be eliminated.
- TBD: +12 VDC at 10 mA may be needed for the noise source. If the noise source can be designed to operate at +5 VDC, then this supply could be eliminated.

3. RF Module Inputs and Outputs

3.1. Data Engine Interface

The RF module is connected to the Data Engine (DE) via an MEC Right Angle 140 pin connector. This connection provides power, clocks, noise source control line, Identification EPROM, and attenuator control to the RF module (inputs) and generates output data samples to the Data Engine. The samples are clocked to the DE at the clock rate of the ADC (122.88 Mb/s rate).

The RF module ADC clock must meet a tight jitter requirement in order to allow the ADC to meet the sensitivity requirement at higher RF frequencies (30 MHz). See the clock module specification.

3.2. Antenna Interface

The connection to the receive antenna is via two SMA receptacles (one per channel) on the module.

The two receiver channels must be clocked by phase-coherent ADC sample clocks. It is recommended that the dual channel unit use signals for the ADC clocks for the two ADC converters that are referenceable to a single common clock in order to maintain tight phase coherence between the two channels. If the ADC clocks between the two channels were to vary with respect to one another, the downconverted baseband phase between them would wander causing degradation or loss of ability to use the two channels for receive polarization control.

While two receive antennas plus the interconnecting cables will have different delays, those are static and can be removed via a one-time calibration. However if the ADC clocks drift relative to one another the resultant phase delay cannot be removed via prior calibration.

The module shall provide an ADC overload output signal for each ADC indicating that the ADC has exceeded its digitization range.

4. RF Module Performance Requirements

The RF module shall meet the following requirements:

4.1. Receiver Noise Figure

The RF module at minimum attenuator setting, and with the filter bypassed shall achieve a Noise Figure of TBD dB across the 100 kHz to 30 MHz range. Note: The Noise Figure is likely to be about 6.5 dB. However the requirement does not need to be this low because the manmade noise level across most of the HF frequency range will be higher. 10 dB or less is probably reasonable, but the requirement is TBD until characterization is completed. If the NF climbs much above 10 dB then noise calibration becomes more difficult as the Excess Noise Ratio (ENR) of the noise source will have to be increased.

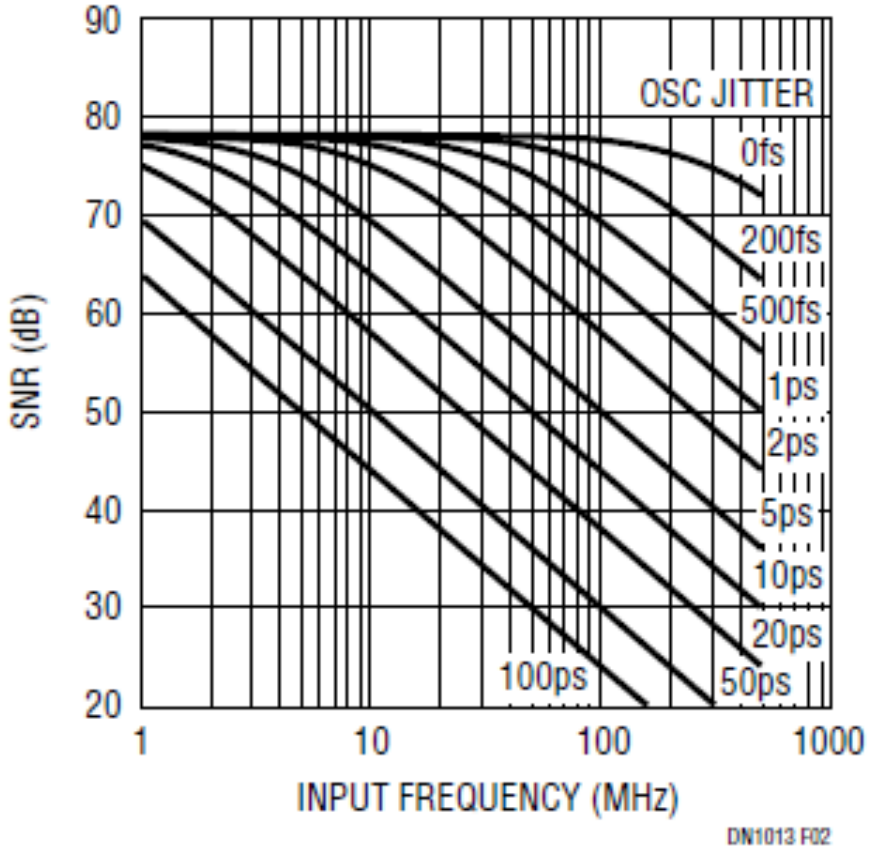
4.2. Dynamic Range

The dynamic range of the receiver shall be specified as the ratio of peak signal to either spurious ADC artifacts, or to 3rd order intermodulation products after the signal has been decimated to bring the ADC noise floor below the spurious or intermodulation products. The objective dynamic range is 80 dB or greater for both ADC spurious and receiver intermodulation products.

4.3. ADC Clock Jitter

The ADC clock shall exhibit less than ±1 picoseconds jitter, peak.

Note: Jitter on this clock degrades the SNR of the ADC conversion. See figure below from a representative ADC specification which graphs this effect. The ADC clock jitter is determined by the Clock Module and its specification. However this receiver module must be careful not to degrade that jitter.



4.4. Clock Phase Noise

The ADC clock input to the RF module shall meet the Phase Noise requirements in the Clock Module specification. Briefly these are:

- The clock and synthesizer phase noise shall be less than -60 dBc at 1 Hz offset, declining as 1/f to less than -120 dBc at 1 kHz offset.

- The phase noise is specified at the NCO frequency of 30 MHz. The NCO is the internal FPGA quadrature down-conversion oscillator. (Since this point is inaccessible, the specification shall be verified by measurement of the resultant baseband signal).
    - Typically the NCO signal will be derived from a higher frequency stable clock by division. Since 30 MHz is the highest specified NCO frequency, it has the smallest division value, and thus should represent the worst case.

4.5. Noise Source and Control

Preliminary: The noise source will provide an Excess Noise Ratio (ENR) of 10.0 dB from 100 kHz to 30 MHz. It may be necessary to adjust the ENR specification to assure that the noise is above the ADC noise level sufficiently. The ENR specification is preliminary until characterization is done.

The RF module shall provide an input binary signal to select / deselect the noise source. When the noise source is DESELECTED, a relay will connect the normal receive signal from the RF input connector to the receiver. When the noise source is SELECTED the relay will connect instead the noise source to the receiver. It is desirable to have the relay function ahead of the attenuator and plug-on filter. This allows using the noise source to verify the attenuator and filter module settings.

A single control bit may be used to switch the noise selection relay for both receivers.

4.6. RF Attenuator and Control

The receiver shall implement a programmable attenuator from 0 dB to 31 dB in 1 dB steps. The attenuator control signals select the value of attenuation. One attenuator per channel is required. The attenuation value for the two receivers shall be independently settable.

4.7. Filter Module

The receiver will be fitted with two sockets on which to plug an optional filter module. One filter module socket per channel shall be provided. The socket can be bypassed if no filter is used. The purpose of the filter is to remove undesired strong signals that would otherwise overload the ADC or degrade the dynamic range of the receiver. For example, an AM Broadcast Band Reject filter may be needed in some locations to prevent ADC overload. Similarly some locations may require a Shortwave reject filter, or an FM/TV Broadcast lowpass filter.

4.8. Data Engine Interface

The receiver will interface to the Data Engine (DE) through a single connector. This interface will be used to support a wide variety of RF Module types, with differing I/O

types. The DE Interface Control Document (ICD) will define the superset of the interfaces. This receiver will implement a specific subset as defined in this module's ICD.

4.9. Identification

The receiver will contain a small EPROM readable through the DE interface that allows the DE to read the type of this module, and identify it as an RXM-5001D.

> Different RF Modules (single and dual receivers, transmitters, and transceivers) will have different I/O signals, signal directions, and functions. The DE will use this identification signature information to load the proper FPGA image to interface to this module type.