HamSCI

Personal Space Weather Station (PSWS)

Clock Module Specification

Preliminary Rev 0.1

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1. Introduction

The Personal Space Weather Station (PSWS) Clock Module provides GPS/GNSS derived time and frequency for input to the PSWS TangerineSDR receiver Data Engine (DE). It is a low cost module that provides a high accuracy pulse-per-second (PPS) timing strobe, high-accuracy UTC time, and programmable frequency synthesizer outputs derived from a GPS disciplined oscillator. The synthesizer outputs have phase noise performance that meets the needs of the PSWS receiver. The module is intended to be programmed from the DE, and to provide timing and frequency signals to the DE. Figure 1 is a block diagram of the Clock Module.

The GNSS/GPS receiver contains a holdover oscillator which continues the phase and frequency outputs when GPS receiver signal is lost. It uses a low-phase-noise oscillator with frequency stability correction.

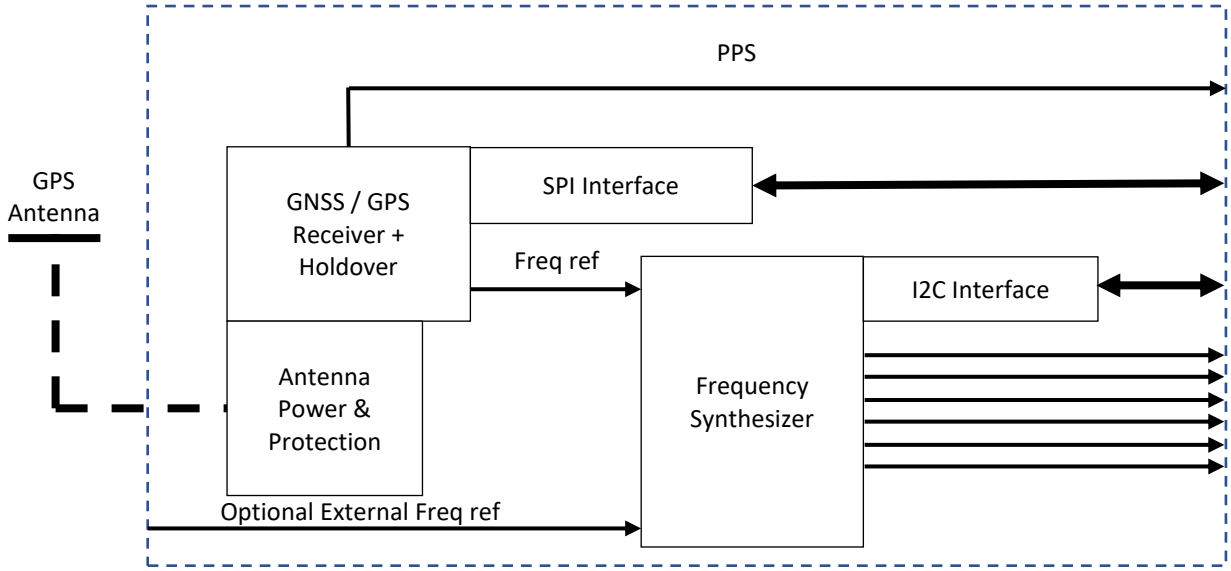

Figure 1. Block Diagram of Clock Module

1.1. Cost Goals

The cost goal of the clock module plus GPS antenna is $100. It is anticipated that higher-performance (perhaps dual RF channel) GPS/GNSS modules may be specified for future use, but likely at significantly higher cost.

2. Power Supply

The Clock Module shall be powered from +3.6 VDC, and shall draw less than TBD mA. The module shall provide DC-power-sourcing protected against short / open to the GPS

antenna coaxial cable (the antenna including an integral low noise preamplifier) via an SMA receptacle.

3. Clock Module Outputs

The clock module provides up to 5 clock outputs that are derived from a GPS/GNSS disciplined frequency. The outputs are:

1. FPGA clock.
2. ADC clock to RF module #1.
3. ADC clock to RF module #2.
4. One Pulse-per-second (PPS) timing output to the FPGA.
5. 10.0 MHz fixed reference output.

The RF module ADC clocks shall come from synthesizer output(s) that guarantee phase stability. These outputs must remain phase coherent across all operating conditions, DC power cycles, and restart conditions. They must utilize a stable distribution method to the DE/receiver modules.

The ADC may supply a source-synchronous data clock back to the FPGA. The clock module may also have a 10.0 MHz reference input when GPS input is not possible. Individual clock outputs shall be able to be deactivated if not used.

****Decision Needed** The electrical format (differential/voltage swing, etc.) and FPGA / ADC clock distribution method is TBD. One possibility is differential LVDS because single-ended clocks are likely to be too noisy across connectors.

The FPGA clock provides the timing to the FPGA, and may provide the ADC clock via clock distribution, or may receive the clock from the ADC via clock distribution. This decision is TBD. Typically this signal will be in the 122.88 MHz range.

The two receiver NCO signals inside the FPGA must hold a constant phase relationship. They cannot be independent oscillators that have a random phase components due to startup phase condition, or programming delay differences.

4. Clock Module Performance Requirements

The clock module shall provide various outputs meeting the following requirements.

4.1. PPS Timing Pulse Accuracy

The PPS timing pulse shall provide better than ± 50 nanosecond peak timing compared to GPS time. This requires the use of a holdover oscillator, which ideally should be within the GPS receiver module itself.

The timing shall meet the requirements in the absence of severe ionospheric disturbances. If there are severe disturbances then timing accuracy will be degraded to ± TBD nanoseconds.

- It is expected that a dual-channel GNSS receiver and antenna combination will be needed to maintain ± 50 nanosecond timing during severe ionospheric events. The cost and performance of that module is outside the scope of this specification and is for a later program phase.

4.1.1. Decimation and Filter Effects

The use of decimation by the HF receiver and DE will cause the samples to be averaged by a CIC and a FIR filter. That filtering process will cause two effects:

1. The sample will be delayed by one-half the FIR filter length, plus the delay of the CIC filter.
2. The CIC filter will cause non-linear phase across the receiver passband which will result in time variation across the receiver passband.

It is expected that the above delays will be constant from unit to unit and will be characterized during engineering analysis of the receiver. An appropriate correction table can be used by the central server if needed to normalize time difference due to decimation. The effects are independent of the PPS, meaning that the PPS timing strobe is not impacted by them, the data samples will be altered and delayed compared to the PPS time strobe due to these effects.

4.2. Frequency Accuracy

The basic frequency accuracy of the 10.0 MHz output shall be TBD parts-per-billion (ppb) during GNSS locked operation, and 100 ppb during holdover operation. The clock module frequency synthesizer shall not degrade the frequency output accuracy of its 6 outputs compared to the reference signal input significantly. The Allan Deviation (ADEV) of the clock module outputs compared against the 10.0 GPS/GNSS clock shall not deviate from the back-to-back ADEV by more than TBD.

- Note: in my measurements of the synthesizer development board, I could not find significant ADEV difference except for a few intentionally-difficult-to-synthesize frequencies.

4.3. ADC Clock

The ADC clock may need to be separately provided or may be provided via clock distribution from the FPGA. The quality of the ADC clock is critical to the performance of the entire PSWS. Excess phase noise decreases the dynamic range of the receiver and

increases baseband jitter, while excess jitter degrades the noise level of the ADC at higher frequencies.

- The ADC clock shall exhibit less than ±1 picoseconds jitter, peak.

4.4. Clock and Frequency Output Phase Noise

The various clock and synthesizer outputs are based on the frequency reference output by the GPS receiver. They should have essentially the same phase noise performance.

- The clock and synthesizer phase noise shall be less than -60 dBc at 1 Hz offset, declining as 1/f to less than -120 dBc at 1 kHz offset.

5. Time Format

The clock module shall provide UTC time to the DE. The DE will use the UTC time and the PPS signal to time-stamp the data samples in the output frame. The intention is to time stamp data samples within ± 50 nanoseconds of GPS/GNSS time.

The DE will format the time to 64-bit NTP format time. This consists of a 32-bit Unix time seconds field, referenced against UTC time, and a 32-bit fractional second field which contains the time value of the first sample in the buffer to within ± 50 nanoseconds.