

Tucson Amateur Packet Radio

Personal Space Weather Station (PSWS)

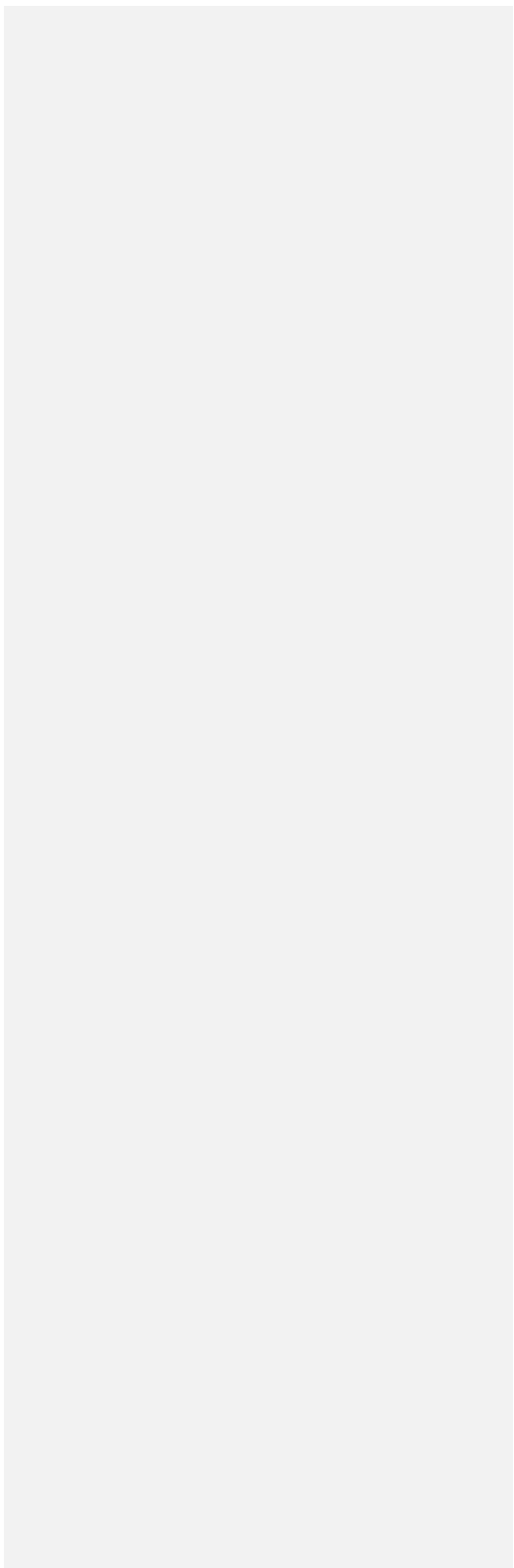
System Specification

Very Preliminary Rev 0.~~2~~4

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1. INTRODUCTION.....	4
1.1. Cost Goals.....	4
1.2. System Components.....	4
1.3. Custom Design vs. COTS.....	5
1.4. Decision Needed.....	5
1.5. Parking Lot / Topics that need to be covered.....	5
2. POWER SUPPLY.....	5
3. CLOCK MODULE.....	6
4. MAGNETOMETER MODULE.....	7
5. RF MODULE.....	7
6. DATA ENGINE.....	8
7. HOST COMPUTER.....	9
8. LOCAL COMMAND AND CONTROL PROTOCOL.....	10
9. REMOTE COMMAND AND CONTROL PROTOCOL.....	10
10. FIRMWARE REQUIREMENTS.....	11
11. SOFTWARE REQUIREMENTS.....	11
12. METADATA SPECIFICATION.....	12
13. FILE FORMAT.....	12
1. INTRODUCTION.....	3
1.1. Cost Goals.....	3

| 1.2. System Components 3



1. Introduction

The Personal Space Weather Station (PSWS) is a low-cost system intended to provide the following functionality:

- Two-channel fully coherent receiver covering 0 – 60 MHz.
- Up to 8 receive frequency slots simultaneously providing up to 192 ks/s each.
- User-pluggable RF filtering to reduce receiver overload in certain situations.
- Programmable 31-step 1 dB RF receive attenuator.
- Amplitude calibration of both receiver channels via an on-board noise generator including RF switching.
- GPS-based receiver providing both accurate timestamping of the received signals and well-controlled receive frequency.
- Integrated 3-axis magnetometer capable of 1 sample/second.
- Gigabit Ethernet interface.
- Storage of up to 24 hours of data in a circular buffer.
- Ability to be remotely polled and to trigger upload of a selected period of previously stored data from the past 24 hours.
- Capable of providing specified metadata.

1.1. Cost Goals

The goal of the project is to produce the receiver portion at a manufacturing cost of \$300. The Magnetometer, receive antennas, data storage, computer control, power supplies, housings, and Internet connectivity functions are not part of this cost goal.

1.2. System Components

The PSWS system is comprised of the following components:

- Data Engine (DE) module.
- Dual-channel receiver module.
 - The DE and RF modules might or might not be combined – TBD.
- 3-Axis Magnetometer module.
- GPS Receiver plus low-jitter and low-phase-noise clock synthesizer module.
- Two receive antennas plus connecting cables, suitably sited. It is recommended that field strength calibration be conducted per site.
- Local host computer with TBD TB of non-volatile storage and a TBD Mb/s connection to the Internet. Initially this is anticipated to be a Single Board Computer (SBC) for example a Raspberry PI 3B+ or an Odroid N2.
- Power supply, power distribution, and equipment enclosure.

1.3. Custom Design vs. COTS

From a specification and operation point of view it is easiest to limit all the components to single specific units. This means that the performance can be well controlled and known, that FPGA firmware has a single variant, and that the software has a single variant. Multiple sources of supply for each component introduces variation in performance (perhaps unknown at the time), and the need for multiple variants of firmware and software.

On the other hand, having multiple sources for each component opens the possibility to enhancements, improved performance, reduction in cost, and alleviation of supply constraints. Additionally the use of pre-existing commercial-off-the-shelf (COTS) hardware and software may reduce the time needed to design, integrate, and test the system solution.

If multiple module realizations are permitted for each functional block, then the number of FW and SW variants needed could grow exponentially. This has the likelihood of making the project unmanageable in terms of on-going development effort and uncontrolled measurement uncertainty.

At the time this specification is written it is too early to tell which approach is required. It is hoped that finalization of the equipment list of materials can be reached and incorporated into this document over the course of the project.

1.4. Decision Needed

Key open decisions are annotated in this document with ****Decision Needed** in the text. These should be decided and documented during the development process.

1.5. Parking Lot / Topics that need to be covered.

Add additional topics that need to be covered here. Move these to appropriate sections as defined and cross-off this list.

2. Power Supply

The PSWS system shall operate from a single external power supply input of +11.0VDC to +15.0VDC (nominally +12VDC). This is desirable in order to allow remotely-powered and battery-backup deployments. All modules and subsystems will need to condition power from this input. If COTS modules are required that cannot utilize +12 VDC as input, then the project will need to design an appropriate voltage step-down and distribution unit. This unit shall provide > 80% power conversion efficiency in order to prevent heat accumulation when deployed in a remote enclosure and to minimize battery backup power consumption (thus extending the run-time hours available per unit of battery capacity).

**** Decision Needed** The unit may be separate, or may be incorporated as a part of another subsystem (such as the data engine). The power consumption from the +12 VDC power input shall be less than TBD amps.

3. Clock Module

The clock module provides up to 4 clock outputs that are derived from GPS. It has a DC-power-sourcing short-protected +5 VDC SMA antenna connector that powers the GPS antenna/preamp, an on-board low-jitter and low-phase-noise multi-channel synthesizer, and up to 4 outputs. The outputs are:

1. FPGA clock.
2. ADC clock to all the RF module(s). This shall come from one synthesizer output, and may utilize any stable distribution method (clock driver per module, or other approach).
- ~~2-3.~~ High-speed reference clock (Scotty: what is this ??)-
- ~~3-4.~~ One Pulse-per-second (PPS) timing output to the FPGA.
- ~~4-5.~~ 10.0 MHz fixed reference output.

The ADC may supply a source-synchronous data clock back to the FPGA. The clock module may also have a 10.0 MHz reference input when GPS input is not possible. Individual clock outputs shall be able to be deactivated if not used.

****Decision Needed** The electrical format (differential/voltage swing, etc.) and FPGA / ADC clock distribution method is TBD. One possibility is differential LVDS because single-ended clocks are likely to be too noisy across connectors.

The FPGA clock provides the timing to the FPGA, and may provide the ADC clock via clock distribution, or may receive the clock from the ADC via clock distribution. This decision is TBD. Typically this signal will be in the 122.88 MHz range.

The ADC clock may need to be separately provided or may be provided via clock distribution from the FPGA. The quality of the ADC clock is critical to the performance of the entire PSWS. Excess phase noise decreases the dynamic range of the receiver and increases baseband jitter, while excess jitter degrades the noise level of the ADC at higher frequencies.

- The ADC clock phase noise shall be less than -60 dBc at 1 Hz offset, declining as 1/f to less than -120 dBc at 1 kHz offset.
- The ADC clock shall exhibit less than ± 500 femtoseconds jitter, peak.

The PPS timing pulse shall provide better than ± 50 nanosecond peak timing compared to GPS time. This requires the use of a holdover oscillator, which ideally should be within the GPS receiver module itself.

4. Magnetometer Module

The magnetometer shall be a 3-axis type, capable of being interrogated at least once-per-second. The magnetometer module shall be interconnected to the system using a TBD interface. (Candidates ~~include but are not limited to:~~ I2C, SPI, RS-422, serial, other).

It may be necessary to physically isolate the magnetometer from the system by a certain distance in order to avoid disturbing the magnetic field in the vicinity of the measuring instrument. The interface shall be capable of both powering and interrogating the module.

The magnetometer shall have less than TBD nanoTesla resolution, and greater than \pm TBD nanoTesla overload.

Cost of the module is a likely a key consideration, although outside the scope of this specification.

****Decision Needed** The actual magnetometer needs to be selected. The electrical interconnection interface, power requirements, and the range and resolution of the magnetometer need to be defined.

5. RF Module

The RF module provides HF receive capability to the system. It amplifies and filters the received signals, and digitizes them. The performance of the RF module is key to the operational capabilities of the entire PSWS. The RF module or modules shall provide:

- Two separate RF channels. The channels shall have better than -30 dB isolation.
- These two channels shall be synchronously and coherently sampled without accumulating or varying phase offset. This requires that the same ADC clock be used for the two converters and that the same NCO signal be used for any downconversion. The use of two NCOs almost always results in uncontrolled difference in the phase of the downconverted signal and is a key problem in many COTs units. If the RF module is separate from the Data Engine, then the NCO requirement is imposed on the DE, not the RF module.
- The RF module shall accommodate a ~~pluggable~~-filter module that is able to accept various filters that may be needed for different receiver locations. The RF module shall also function with no filter. The ~~filters might~~se may include:
 - AM Broadcast band rejection
 - SW station rejection.
 - FM Broadcast rejection.

- The RF module shall have programmable attenuation in the front end to reduce the possibility of ADC overload that can occur in some situations.
- The RF module shall provide at least 14 bits ADC resolution. The actual ENOB of the converter is TBD.
- The RF module shall provide less than 10 dB noise figure when no attenuation is selected.
- The RF module shall provide greater than 88 dB dynamic range for directly-sampled (unconverted) signals. This is defined as the ratio of the maximum allowable signal to the spurious and/or 3rd order signal(s) which are likely below the ADC noise floor and thus might only be uncovered after averaging or equivalent. Downconversion and decimation within the DE will increase the dynamic range due to bandwidth reduction.
- A noise generator that can be switched into ~~the~~each RF antenna paths for generating a known amplitude signal level to be used for calibration.

****Decision Needed** Whether the RF module is separate or integrated with the Date Engine. This is primarily a decision of purpose-built vs. COTS implementation.

6. Data Engine

The Data Engine (DE) provides the electrical signals to control the receiver, and possibly the Magnetometer (although that could ~~theoretically also~~ be controlled by the Host computer instead). It converts the ADC samples to packetized information. It provides a mechanism to mark low-level metadata within the packets. It provides a control interface to the host computer for setting frequencies and downconversion parameters.

The DE contains a programmable FPGA due to the high sample rates and precision timing needed. It contains a 1 GE Ethernet interface to the host computer. It provides data processing for 2 RF channels.

The DE connects to the clock module to receive FPGA clock, ADC clock, and PPS timing mark.

The DE shall provide downconversion, filtering, and decimating up to 8 RF bands of 192 kHz bandwidth per RF channel.

The DE shall provide low-level metadata marking in the data packets consisting of:

1. Identify which RF channels the samples are from.
2. Identify which RF band (if downconversion is enabled) that the samples are from.
3. Identify the sample rate of the RF band.
4. Identify if there is a PPS mark in the packet, and if so:
 - a. Which sample number it applies to.
 - b. The GPS second of the PPS mark.

5. Identify whether the data consists of received signal samples or amplitude calibration samples.

The host computer is responsible for higher-level metadata marking, and potentially the file encoding format (TBD).

If the DE and Host are physically separate devices, then the DE may need to stream data directly to the central server if the Host cannot process fast enough.

7. Host Computer

The host computer is responsible for:

- Controlling the DE, i.e. setting the RF bands and attenuator.
- Processing received Ethernet packets from the DE.
- Applying high-level metadata to the packets.
 - Metadata version marking
 - Frequency, time and date of the data.
 - SiteID or other data (such as GPS coordinates) of the receive antennas.
- Storing the Packets in a 24-hour circular buffer.
- Receiving commands via the Ethernet interface.
 - Remotely via the Internet, and
 - Locally via a Web interface.
- Transmitting the data to a central server upon request.

** Decision Needed

- Still to be determined is whether the Host computer will provide file formatting such as Digital RF / HDF5 format, or whether the central server will perform that conversion. The issue is that the Host may not be able to keep up in real time with HDF5 encoding due to the very high processing load.

The Host computer shall provide a 1 GE Ethernet interface.

** Decision Needed

- Still to be determined is whether the DE or the Host will interface to, collect, and format the data from the Magnetometer module.

The Host computer shall provide sufficient local non-volatile storage to hold 24 hours of received samples. The exact amount of storage needed is not completely defined at this point, but can be estimated by:

86400 seconds	(24 * 60 * 60)
6.144 Ms/s	(2 RF chan * 8 RF band * 192000 samples/sec * 2 (I+Q))
4 bytes/s	(single precision floating point)

= 2.13 Terabytes

The non-volatile memory interface data sample rate can be estimated as:

6.144 Ms/s sample rate
 4 bytes / sample
 few bytes metadata per packet

= Roughly 25 Megabytes / sec.

This requires SATA-2 or higher hard disk interface performance. It is unlikely that USB2 memory could handle this data rate on a sustained basis.

8. Command Local Command and Control Protocol

The protocol between the DE and Host is called the Local Command and Control protocol. This is used by the host to set the DE mode of operation, and control the subtended modules (i.e. the RF receiver, Magnetometer, and others). It also communicates the status of the controlled units back to the host.

At this point the protocol is not defined, and will await further development, and probably will be dependent on any COTS modules selected for the PSWS.

The protocol shall be covered in a separate specification. The LCC Protocol specification should cover at a minimum:

- Protocol revision control, revision marking and reporting.
 - Including GitHub or other revision control
- Description of all HW modules utilized and controlled.
- Reference to the Low level metadata specification.
- Command and Control interface.
- Status interface.
- Reference to the packetization definition.

9. Remote Command and Control Protocol

The protocol between the Host and the Central Server is called the Remote Command and Control Protocol. Because this protocol will be carried over the public internet, it must be capable of being secured against unauthorized use. What type of security and authentication is necessary is TBD. The purpose of the protocol is for the central server to be able to:

- Establish the operating parameters of the PSWS, such as bands tuned, sample rate, attenuator setting, etc.
- Trigger the retrieval of data covering a time in the past that is within the PSWS buffer on non-volatile storage.
- Negotiate the file format (whether the host or the server does file encoding, etc.)

- Identify the remote station and confirm.
- This protocol is likely subject to frequent revision as the project needs evolve.

The protocol shall be covered in a separate specification. The RCC Protocol specification should cover at a minimum:

- Protocol revision control, revision marking and reporting.
 - Including GitHub or other revision control
- Reference to the High level metadata specification.
- Reference to the File format specification if the Host does file encoding (such as Digital RF / HDF5).
- Command and Control interface.
- Status interface.

Firmware is defined to be the FPGA code that is deployed on the DE module. This shall be covered in a separate specification due to the size and complexity anticipated. The FW spec should cover at a minimum:

- FW Revision control, revision marking and reporting.
 - Including GitHub or other revision control
- Hardware interface definition for the FPGA.
- Block diagram.
- Low level metadata applied.
- Command and control interface.
- Status interface.
- Packetization process.
- External modules used (Protocol stack, GE interface, filters, etc.).
- Toolchain utilized, including versioning.

11. Software Requirements

Software is defined to be the Host source code. This shall be covered in a separate specification due to the size and complexity anticipated. The SW spec should cover at a minimum:

- SW Revision control.
 - Including GitHub or other revision control method.
- SW Architecture document.
- High level metadata applied.
- Command and control interfaces:
 - To the DE,
 - To the Internet,
 - To a local Web client.
- Status interface.
- Toolchain utilized, including versioning.

- Non-volatile memory storage.
- Interface to the Internet or modem/switch/gateway (Layers 2 and 3).
 - Including DHCP, Firewall, VPN, etc. as needed.

12. Metadata Specification

The metadata is split into two portions:

- Low-level metadata (applied by the DE).
- High-level metadata (applied by the host).

The metadata shall be defined by a separate specification. Critical to this specification is revision control, revision identification, and revision marking of the data. It is anticipated that the metadata will change on a research-by-research project basis. As each new research activity needs to identify some differing (and at the present unknown) attribute of the data, the metadata will likely change.

Additionally, as new hardware is added or changed out to accommodate new research requirements, the metadata formats applied will also likely change. This includes the identification of the hardware version producing the data, as the resolution, accuracy, and range of the new hardware may differ significantly from older hardware.

Each data packet sent to a central server needs to be annotated with metadata, and with metadata version identification if it is to be utilized in the future. It defines the ability to accurately curate the archived data long-term. If key attributes of the data are unknown 5 or 10 years hence, the archived data may be of little use.

13. File Format

The information archived by the central server should be in a readily-accessible standard format. One example is the Haystack Digital RF / HDF5 container set of standards.

As previously described, it is still undecided whether that file format conversion happens in the Host computer or in the Central Server. If the later, then the Host computer needs to provide sufficient information to the central server to accurately translate the information to the desired file storage format.

It is anticipated that the file format is adequately specified elsewhere, and shall be included by reference in this document.