Tucson Amateur Packet Radio

TangerineSDR inexpensive Data Engine (TiDE)

Hardware Specification

Preliminary Rev 0.1

24 April 2019

1. Introduction

The TangerineSDR is a modular FPGA-based Software Defined Radio. It is built on several PCB modules: a Data Engine baseboard, one or two plug-in RF Modules and a plug-in Clock Module. The Data Engine (DE) baseboard (Figure 2) contains a 4-channel low-speed DAC and an FPGA (the FPGA contains an internal multi-channel slow-speed ADC.) It has a three-port Gigabit Ethernet switch, with one port connected locally to the FPGA and the other two connected to RJ-45 jacks for external connections. One external port is for connection to a Single Board Computer (SBC) for SDR Command and Control and the other is for connection to a local LAN or Internet gateway for direct streaming of data. It has a full-duplex SuperSpeed USB 3.0 (full duplex 5Gbps) device interface and a micro-SDXC card slot for local buffering of data. It also has a High-Speed USB 2.0 Host port for a USB memory stick or a DVB radio dongle.

With appropriate RF modules, the TangerineSDR can be used as a Personal Space Weather Station (PSWS) receiver, a satellite communications radio (for example, a Phase 4 ground station), as well as a general-purpose Software Defined Radio transceiver.

The TangerineSDR can be configured as receive-only, using one of the two RF module connectors for an RF receiver (RX) module, or as a transceiver using one RF module connector for an RX module and the other for an RF transmitter (TX) module. The two RF module connectors are arranged along one axis, allowing a double-wide transceiver module (TRX) to be used with the DE board. The intent of this modular approach is to support multiple widely disparate RF functions with one FPGA-based Data Engine.

Power is supplied to the DE from an off-board 11V - 15V power supply or by a 12V battery. The power input is rated at 19V maximum and 11V minimum. Power and clocks are supplied to the RF Module connectors via the DE baseboard.

While the information in this section applies to the entire TangerineSDR system, sections 2 and 3 describe only the Data Engine hardware. For Clock Module information, see the document **TangerineSDR Clock Module Specification** and for RF Module information, see the document **TangerineSDR RF Module Specifications**.

Additional information is contained in the documents **TangerineSDR UDP Protocol**, **TangerineSDR RF Module Interface Specification** and **TangerineSDR Command and Control Network Protocol**.

1.1. Design Goals

1.1.1. Personal Space Weather Station (PSWS) Receiver

The Personal Space Weather Station (PSWS) receiver RF Module has a receive range of 100kHz through 60MHz. Along with external sensors connected to either the DE or its attached SBC, it is useful for collecting ionospheric sounding and other solar data. Two channels are synchronously sampled at 122.88Msps by a dual 14-bit ADC. The PSWS RX Module has an on-board noise source that provides a known signal level used to calibrate the receiver. A 31-step, 1dB resolution attenuator controlled by the DE board provides AGC hardware to help prevent RF overload.

1.1.2. Phase 4 Ground (P4G) Station

The RF Modules for Phase 4 Ground station support are ****TBD****. The P4G station consists of a 10GHz receiver and a 5GHz transmitter. The receiver will likely be a 900MHz LNB at the antenna, followed by a 900MHz SAW filter ahead of an under-sampled receiver operating in the 15th (860 – 920MHz) or 16th (920 – 980MHz) Nyquist band.

The transmitter will likely be a baseband design, with up-conversion and power amplification at the feed horn of the antenna.

1.1.3. SDR Experimenter's Platform

The RF Modules for experimenters' use are ****TBD****, although the PSWS receiver RF Module may be used for this purpose.

1.1.4. General Purpose Software Defined Radio

The RF Modules for general purpose use are ****TBD****, although the PSWS receiver RF Module may be used for this purpose.

1.2. Cost Goals

The following cost goals are based on a build lot size of 1000 units and are actual build costs. Sale prices can be 30% to 50% higher or more, depending on retail sales arrangements.

1.2.1. Data Engine (DE)

Cost goal for the TangerineSDR DE is $150, including BOM, PCB, assembly and test costs.

1.2.2. PSWS RX Module

Cost target for the PSWS RX Module is $100, including BOM, PCB, assembly and test costs.

1.2.3. Phase 4 Ground RX and TX Modules

Costing for the P4G RX and TX Modules is ****TBD****.

1.2.4. Future RF Modules

Costing for future modules is obviously ****TBD****. The TangerineSDR DE will support very high data rates, especially if the RF Module is configured for supported LVDS data communication. Higher performance modules will cost more but will be fully supported by the same DE within the constraints of FPGA resources.

1.3. I/O, Shields and Compatibility

The TangerineSDR DE is compatible with existing expansion boards: Raspberry Pi Hat/Micro Hat, Arduino Shield, mikroBUS™ (Click™) board, Ultra96 Mezzanine and Digilent Pmod™ modules. It is also able to act as a shield itself to Raspberry Pi 3, Odroid N2 and compatible Single Board Computers (SBCs).

1.3.1. Raspberry Pi and Odroid SBC Connectivity

The Tangerine DE has a 40-pin male header on the top side, and a 40-pin female receptacle on the bottom side. This allows the DE to be used as a hat by plugging it onto an RPi, Odroid or other SBC. The top header allows a standard hat to be plugged into the DE as well. Since all of the digital I/O pins are programmable, either or both configurations are supported.

The standard RPi hat is 65x56.5mm, with a 40-pin, 2.54mm pitch, dual-row connector along the top edge. The Micro-Hat uses the same connector, but the board measures 65x30mm.

1.3.1.1. Tangerine DE as a Hat

The DE may be configured as a base board, communicating with standard (or custom) hat boards via I2C, I2S, SPI, UART and/or GPIO ports. In this configuration, the DE acts as an SBC talking to a hat board.

1.3.1.2. Tangerine DE as a Base Board

The DE may be configured as a hat board, communicating with SBCs via I2C, I2S, SPI, UART and/or GPIO ports. In this configuration, the DE acts as a custom hat controlled by an SBC board.

1.3.1.3. Tangerine DE as Both Base and Hat Boards

The DE may alternatively be configured as both a base board and a hat. In this configuration, some of the I2C, I2S, SPI, UART and/or GPIO ports communicate with one or more standard (or custom) hat boards, while other ports communicate with the attached SBC. In this configuration, the DE acts both as an SBC talking to a hat board and a custom hat controlled by the DE. Some of the shield pins may simply pass through, allowing the SBC to control the hat(s) directly, without DE intervention.

1.3.2. Arduino Shield

Arduino shields are typically 68.6x53.4mm. The TangerineSDR has space for one Arduino shield on top of the board. They typically have long connector tails and may be stacked. The shield connectors consist of two 0.100” pitch single-row receptacles (an 8-pin and a 6-pin on the left edge, and an 8-pin and a 10-pin along the right edge). IN addition, a 6-pin SPI programming port is located along the bottom edge of the board.

1.3.3. mikroBUS™ (Click™) Board

A small mikroBUS™ board, commonly referred to as a Click board™ measures 28.6mm long by 25.4mm wide. The Click™ board interface connectors (two 8-pin 0.100” pitch single-row receptacles) sit between the Arduino shield connectors, so a Click board™ may only be used when no Arduino shield is fitted. Provision for medium (42.9mm long) and large (57.15mm long)

1.3.4. Ultra96 Mezzanine Board

The Ultra96 board mezzanine connectors consist of a 40-pin low-speed 2.0mm pitch receptacle and a 60-pin high-speed Bergstak 0.8mm receptacle. The ultr96 board footprint is 85mm long by 54mm wide, and mezzanines come in many different sizes. Additional board space on mezzanine cards is usually made by extending the left edge of the card. Placement of the Ultra96 Mezzanine connectors will allow the left mezzanine board edge to extend past the nearest DE board edge. Ultra96 mezzanine boards will not overlap the Arduino shield/Click™ board area, allowing both to be used simultaneously.

1.3.5. Digilent Pmod™ Modules

Pmod™ connectors are right-angle, 12-pin dual row 0.100” receptacles located near a board edge. They are separated by enough distance to allow both connectors to be used at the same time. Pmod™ boards are typically 0.8” wide, but a wider spacing should be used on the DE board, if possible, to accommodate wider boards.

1.4. System Architecture

Due to the limited capabilities of the SBC in most systems, a somewhat different system architecture is employed from a conventional SDR where the SBC is in the middle of the data path. The SBC will perform authentication and present a command and control interface to the network via its TCP/IP stack. The SDR hardware is then controlled by the SBC using an SDR-local UDP protocol. The SDR-local protocol is not exposed to the network outside the SBC-SDR connection for security reasons. The SBC can set up direct high-speed UDP paths to and from the SDR hardware. While the endpoints of these UDP streams can be outside the local network, the streams themselves can only be set up by the SBC under the TCP/IP command and control protocol. Since the SBC will be running an operating system (Linux assumed), security will be implemented within the framework of that operating system. The system configuration is shown in **Figure 1**.

Note that if more processing power is required in the system, the SBC may be replaced by a more powerful computer. All that is required on the local computer is a GbE port. In some systems, the SBC may do some local processing, but still require larger proceeding power or more storage. UDP streams may be directed to any needed network resource, either on the local network segment or out on the Internet.

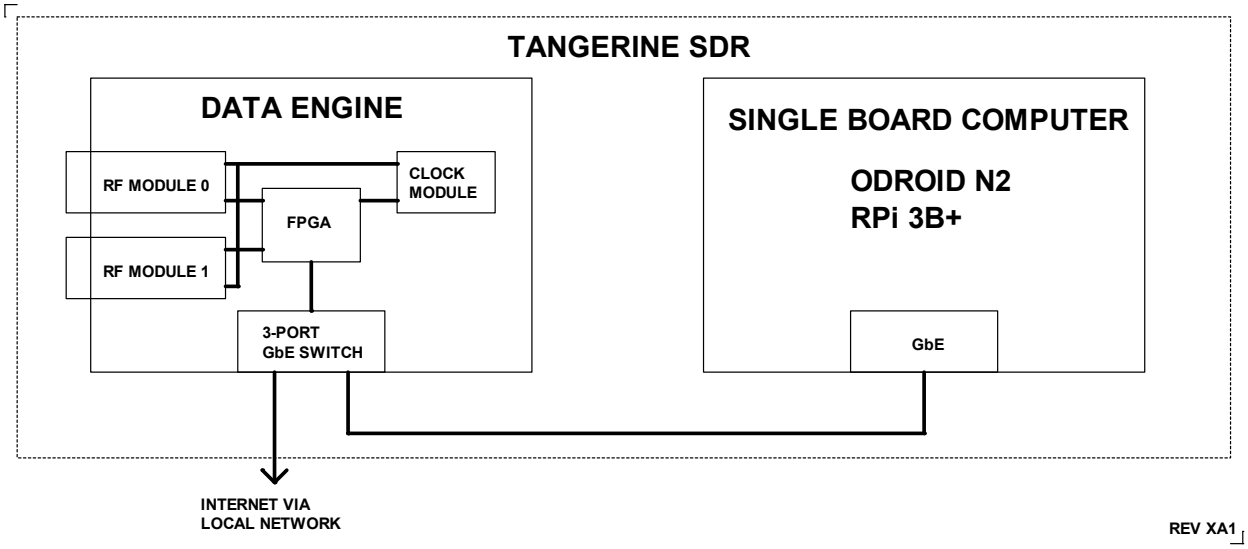

Figure 1 TangerineSDR System Block Diagram

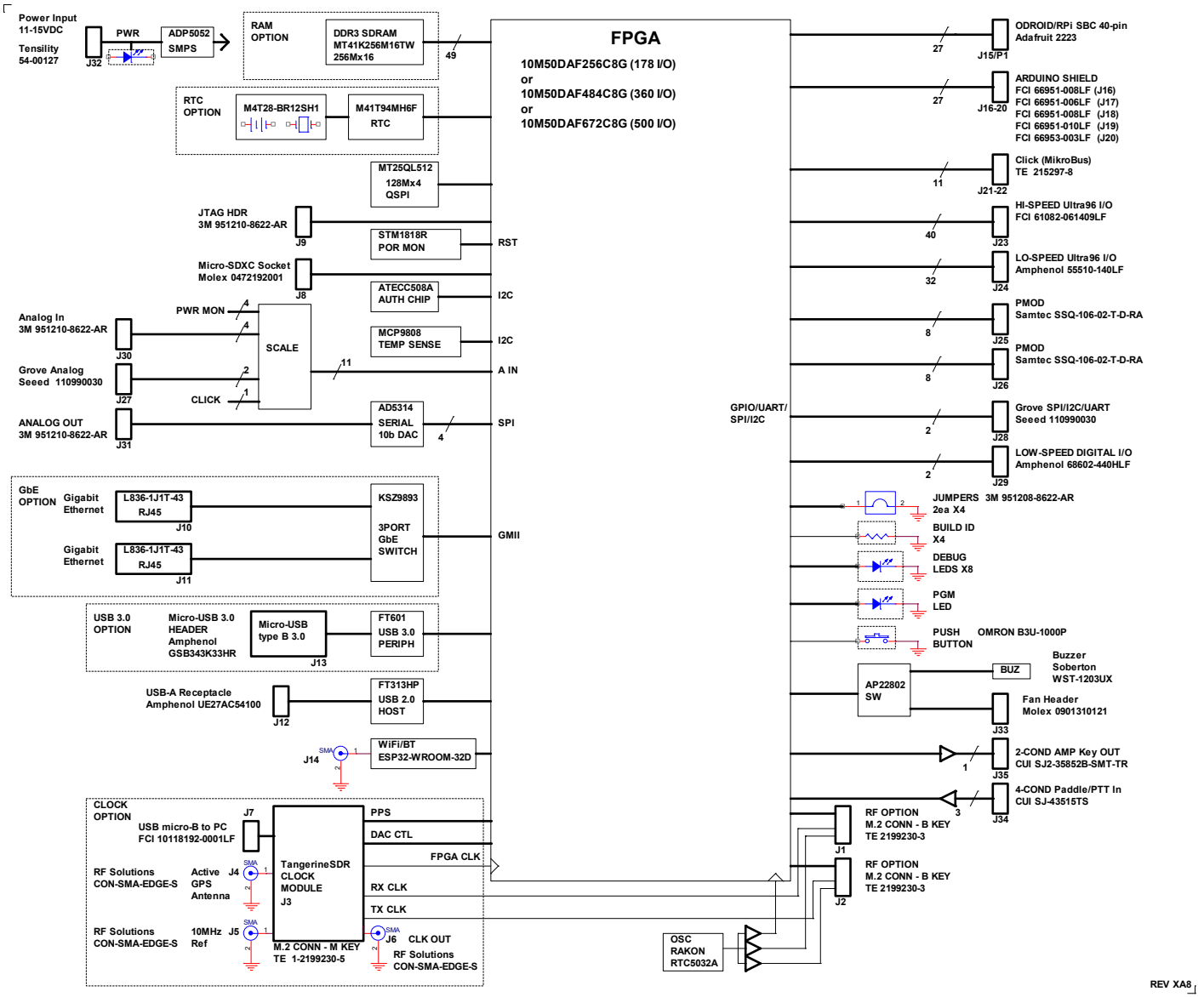

Figure 2 TangerineSDR Data Engine Block Diagram

2. TangerineSDR Data Engine (DE) Hardware Description

2.1. RF Module Ports

The RF modules are mounted on B-keyed M.2 NGFF plug-in PC boards. The two connectors on the DE have equivalent I/O connections, so any RF module may be plugged into either connector. Both RF module connectors are mounted on the same axis, allowing a double-RF module to be plugged into both connectors simultaneously. The double-RF module can thus access twice as many I/O pins as a single card to accommodate high pin-count functions.

Each RF module connector has both 5V power and 3.3V power, as well as both differential LVDS and single-ended I/O pins. Four pins on each module connector are reserved for an ID function, allowing the FPGA to identify 15 different installed module types, as well as empty slots.

See the document **TangerineSDR RF Module Interface Specification** for more information.

2.2. Clock Module Port

The oscillator and/or GPS are supplied by a clock module mounted on a Bd M.2 NGFF plug-in PC board. The clock module produces four independent clock outputs. Three of these drive the FPGA and the two RF module ports, while the fourth one drives an SMA connector for off-board uses. All the clock module I/O pins are connected either to the FPGA or to SMA connectors for external use. The clock module has a control port (I2C or SPI) that connects to the FPGA for clock programming and control.

See the document **TangerineSDR Clock Module Specification** for more information.

2.3. FPGA and Support Circuitry

The FPGA is an Intel/Altera MAX10 device, part number 10M50DAF256C8G in an FBGA256 package. This package provides 178 GPIOs, including 13 LVDS transmitter pairs and 80 LVDS receiver pairs.

Alternate MAX10 part numbers are 10M50DAF484C8G with 360 GPIOs, 24 LVDS transmitter pairs and 171 LVDS receiver pairs or 10M50DAF672C8G with 500 GPIOs, 30 LVDS transmitter pairs and 241 LVDS receiver pairs. These two parts offer many more I/O pins but cost more. An alternate will only be used if the larger number of I/O pins is needed.

All three of the MAX10 variants above provide an FPGA solution with 1.6Mbit of on-board RAM memory, 144 18x18 multiplier blocks and two 10-bit ADCs. A Gigabit Ethernet MAC, SPI, I2C and UART ports are implemented in FPGA fabric.

A JTAG programming/debug port is provided for connection to a USB Blaster or equivalent. This port is used to program the MAX10 internal flash memory and the external QSPI flash memory. It is also used to run the Altera SignalTap hardware debugger.

2.3.1. SDRAM Memory option

A single SDRAM part, Micron MT41K256M16TW provides 512Mbytes of DDR3L memory, arranged as 256Mx16. This part can be made optional to reduce cost. The RAM can be used to store a NIOS run-time image or for data buffering.

2.3.2. QSPI Flash Memory

The DE contains a single-chip 512Mbit (64MByte) QSPI flash memory, Micron part number MT25QL512ABB1EW9-0SIT. If this part is not available, an alternate 256Mbit part is compatible, part number MT25QL256ABA1EW9-0SIT. This 512Mb memory is arranged as 1024 sectors of 64KBytes each and can be used as a buffer for update decryption or other uses. The 256Mbit memory is arranged as 512 sectors of 64KBytes each.

2.3.3. SDXC Card Memory Slot

The DE contains one slot supporting SDXC cards of up to 2TB. This memory can be used to store either raw I/Q data or processed data. Supported write speed is ****TBD****.

2.3.4. Crypto Authentication

A Microchip ATECC508A crypto authentication chip provides a resource to run public key algorithms. It connects to the FPGA via an I2C interface.

2.3.5. Real Time Clock (RTC) option

The RTC is an ST Microelectronics M41T94MH6F and is used to keep real time in the absence of external power. Real time can be adjusted from the Internet via the Ethernet port and a time service such as NIST. A M4T28-BR12SH1 snap-hat contains a 32.768kHz crystal and a 48mAh lithium backup battery to power the RTC when power is absent. It is snaps onto the RTC chip for easy replacement. Battery life is estimated to be in excess of 5 years. The RTC and battery can be made optional to reduce cost.

2.3.6. Temperature Sensors

The DE board supports a pair of temperature sensors. An on-board MAX10 internal temperature sensor can be read using one of the MAX10's 12-bit ADCs. This sensor may be used to report MAX10 die temperature or for fan control.

The other temperature sensor is a Microchip MCP9808, connected to the FPGA via an I2C interface. This sensor may be used to report ambient temperature or for fan control.

2.3.7. Power-on Reset

A power-on reset is generated by an ST Microelectronics STM1818R power supply monitor. It holds the reset pin active until approximately 2μs after Vcc reaches 2.55V.

2.1. Communications Ports

There are four types of communications ports on the DE: Gigabit Ethernet (GbE), USB 2.0 host port, USB 3.0 device port and WiFi.

2.1.1. Gigabit Ethernet Ports

The DE contains a three-port gigabit Ethernet switch, implemented with a Microchip KSZ9893. One port connects to the FPGA, while the remaining two connect to on-board RJ45 jacks.

2.1.2. USB 2.0 Hi-Speed Host Port

One Hi-Speed USB 2.0 host port is implemented with an FTDI FT-313H USB embedded host controller. An on-board USB type-A receptacle is fitted to the DE board. The intended use of this interface is to connect a DVB SDR dongle.

2.1.3. USB 3.0 SuperSpeed Peripheral Port

One SuperSpeed USB 3.0 peripheral port is implemented with an FTDI FT-601 USB-to-FIFO part. An on-board USB 3.0 type micro-B connector is fitted to the DE board.

2.1.4. Wi-Fi and Bluetooth option

The DE uses an Espressif Systems ESP32-WROOM-32D module for 802.11b/g/n Wi-Fi and BT 4.2 capability. The WiFi module has a connection for an optional external antenna.

2.2. Expansion Ports

Six standard expansion ports are provided: an SBC (e.g, RPi 3B or Odroid N2) host/shield, an Arduino shield, a mikroBUS™ Click™, an Ultra96 mezzanine, and two Pmod™ ports. One general-purpose low-speed I/O header provided additional un-assigned I/O ports.

2.2.1. SBC Hat and Host Interface

A 40-pin female socket is mounted on the back of the DE board, opposite a 40-pin male header on the top side. This arrangement allows the DE board to be used as an SBC hat, as a host to an SBC hat, or as both at the same time. The connections on the bottom socket are passed through to the pins on the top header to even allow the SBC (mounted below) to have direct control of the hat (mounted above). Since the FPGA pins are programmable in function and direction, all configurations are possible.

2.2.2. Arduino Shield

One Arduino-compatible set of shield connectors is provided. This will allow nearly any existing Arduino shield to be installed on the DE board. Custom shields designed specifically for the TangerineSDR DE board are also supported. Shields can provide many types of low-speed interfaces limited only by the number of shield pins and FPGA resources. Only top-mounted sockets are provided; no pins extend below the DE PCB.

2.2.1. mikroBUS™ Click™

Nested between the Arduino shield connectors is a mikroBUS™ standard interface for a Click board™. Since it is located within the Arduino shield footprint, it can only be used if an Arduino shield is not fitted.

2.2.2. Ultra96 Mezzanine

Thirty-two low speed I/O pins are provided on a 40-pin expansion connector, and forty high speed I/O pins are provided on a 64-pin expansion connector. The low-speed connector supplies 5V power, I/O power, and low-speed I/O ports, while the high-speed connector provides high-speed I/O ports only. The low-speed I/O and high-speed I/O connectors are physically placed to allow Ultra96 mezzanine expansion boards to be fitted.

2.2.1. Pmod™ Ports

Two Pmod™ headers are provided on the DE. These headers can be configured to use I2C, SPI or UART interfaces in the FPGA. These are intended to be used for low-speed devices, such as sensors.

2.2.1. Grove I/O

Two 4-pin Grove connectors are provided, one for analog connections and one for digital connections. The analog connector provides two analog inputs to the FPGA ADC. The digital connector provides two digital I/O connections to the FPGA. The digital I/O pins can be configured as an I2C or UART port, or GPIO pins. Both Grove connectors also supply both +3.3V and ground connections.

2.2.2. Low-Speed Digital GPIO

An additional header is mounted on the top side of the DE to provide additional 3.3V digital GPIO pins to control off-board logic. The connectivity will likely be to ribbon cables routed to additional boards in a system.

2.2.3. Analog I/O

The DE board supports 4 analog inputs and 4 analog outputs.

2.2.3.1. Analog Inputs

Four analog inputs are routed to one of the MAX10's two internal ADCs. This ADC is a 12-bit converter that can run as fast 1 Msps. Scaling and protection circuits allow each input to safely handle 0 to +3.3V levels with ESD protection.

2.2.3.2. Analog Outputs

Four analog outputs are produced by an ADI AD5314 10-bit DAC. It interfaces to the FPGA via a SPI port at up to 30MHz serial data rate. Optionally, an AD5324 12-bit DAC can be fitted in place of the AD5314 10-bit DAC to give the outputs more precision. This DAC has an 8µs settling time and an approximate update time of 600ns. This yields a maximum conversion rate of about 100kHz.

Each analog output has a range of 0 to 3.3V.

2.3. Power Supplies

The DE operates from a single external power supply input of +11.0VDC to +15.0VDC (nominally +12VDC) at less than 4A. From this 12V input, an ADI ADP5052 SMPS regulator generates multiple voltages. The input power is supplied through a 5.5mm OD, 2.1mm ID coaxial power connector.

The DE on-board SMPS regulator voltages are listed in Table 1. Note that the maximum current values are regulator maximum specifications and not power consumption values. A block diagram is shown in Figure 3.

Supply	Max Current	Regulator P/N	Used for
+11.0V to +15.0V	4A		Input power supply
+5.0V	4A	ADI ADP5052	TX and RX Option Modules
+3.3V	4A		MAX10 I/O, LEDs, Analog, µSDHC
1.2V	1.2A		MAX10 PLL digital, GbE
1.2V	1.2A		MAX10 core
2.5V	200mA		MAX10 PLL analog

Table 1 Data Engine SMPS maximum current ratings

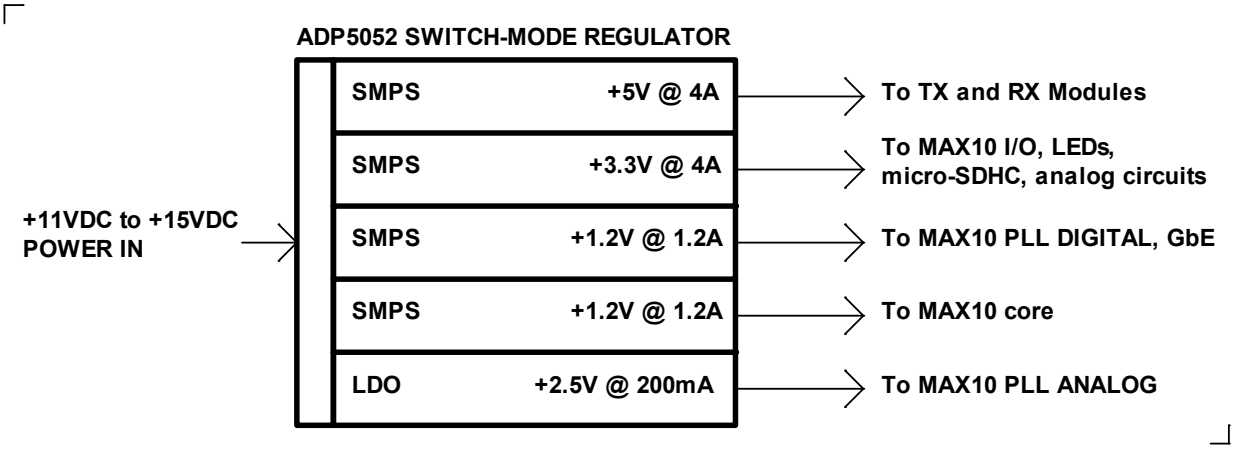

Figure 3 Data Engine Power Supply Block Diagram

2.3.1. Power Consumption Estimates

Table 2 shows the major DE power-consuming components and their power requirements. Total DE maximum power dissipation is projected to be under 25W.

Component	5.0V	3.3V	2.5V	1.2V PLL	1.2V Core
FPGA	-	1A	200mA	200mA	1A
QSPI flash	-	50mA	-	-	-
Serial DAC	-	5mA	-	-	-
Ethernet KSZ9893	-	200mA	-	500mA	-
Fan	-	100mA	-	-	-
LEDs	-	90mA	-	-	-
clock module	500mA	-	-	-	-
RF modules	2A	2A	-	-	-
total	2.5A	3.5A	200mA	700mA	1A

Table 2 Power consumption estimates

2.4. System Resources and I/O

2.4.1. Jumpers

Eight jumpers are provided that can be read by logic within the FPGA (e.g., a NIOS soft-core CPU). Currently these are not defined. When a jumper is placed, the corresponding FPGA input is low. Definitions are shown in Table 3.

Jumper name	Signal name and ON state	Indicates
JP0	low when JP0 is placed, high when not placed	firmware defined
JP1	low when JP1 is placed, high when not placed	firmware defined
JP2	low when JP2 is placed, high when not placed	firmware defined
JP3	low when JP3 is placed, high when not placed	firmware defined
JP4	low when JP4 is placed, high when not placed	firmware defined
JP5	low when JP5 is placed, high when not placed	firmware defined
JP6	low when JP6 is placed, high when not placed	firmware defined
JP7	low when JP7 is placed, high when not placed	firmware defined

Table 3 Jumper Functional Definitions

2.4.2. Build I.D. Straps

Four zero-ohm resistors are provided to be installed at build time to install various build options. These allow 16 identifiable build variants, shown in Table 4.

ID3	ID2	ID1	ID0	Description
0	0	0	0	Build variant 0: TBD
0	0	0	1	Build variant 1: TBD
0	0	1	0	Build variant 2: TBD
0	0	1	1	Build variant 3: TBD
0	1	0	0	Build variant 4: TBD
0	1	0	1	Build variant 5: TBD
0	1	1	0	Build variant 6: TBD
0	1	1	1	Build variant 7: TBD
1	0	0	0	Build variant 8: TBD
1	0	0	1	Build variant 9: TBD
1	0	1	0	Build variant 10: TBD
1	0	1	1	Build variant 11: TBD
1	1	0	0	Build variant 12: TBD
1	1	0	1	Build variant 13: TBD
1	1	1	0	Build variant 14: TBD
1	1	1	1	Build variant 15: TBD

Table 4 Build ID input Definitions

2.4.3. LEDs

There are nine LEDs on the DE. LED functions are listed in Table 5, along with the conditions on which they are lit. They are all active-high outputs, i.e., the LED is lit when the output is high.

LED name	LED color	Signal name and ON state	Indicates
done	green	off when FPGA is uninitialized	unprogrammed, done LED off
		on when FPGA is initialized	normal, done LED on
LED0	red	off when LED0 is low, on when high	firmware defined
LED1	red	off when LED1 is low, on when high	firmware defined
LED2	red	off when LED2 is low, on when high	firmware defined
LED3	red	off when LED3 is low, on when high	firmware defined
LED4	green	off when LED4 is low, on when high	firmware defined
LED5	green	off when LED5 is low, on when high	firmware defined
LED6	green	off when LED6 is low, on when high	firmware defined
LED7	green	off when LED7 is low, on when high	firmware defined

Table 5 LED Functions

2.4.4. Push Button

One momentary push button is provided. De-bouncing must be done in FPGA hardware. The switch part number is Omron B3U-1000P.

2.4.5. Buzzer

A 3.3V buzzer is provided. It is a Soberton part number WST-1203UX, and is switched by a Diodes, Inc AP22802.

2.4.1. Fan

A two-pin fan header provides 5V power to an external cooling fan. This power can be switched on or off by an FPGA logic output by a Diodes, Inc AP22802. The output is rated at 1A.

2.4.2. Buffered PTT/Paddle/Amp Key I/O

Two jacks are provided for three protected digital inputs and one buffered digital output. The input jack is a 4-pin 3.5mm audio type for electronic keyer paddle input and microphone PTT input. The output jack is a mono 3.5mm audio type to key an RF power amplifier. The inputs are pulled up to 5V, and the output is rated at 60V@100mA sink current.

3. TangerineSDR Data Engine Connectors and Pin-outs

3.1. M.2 RF Module Connectors

The RF Module connectors are 67-pin NGFF receptacles. The connector is a TE p/n 2199230-3 B-Keyed M.2 connector. The pin out is shown in Table 6.

J1/J2 pin #	Pin Name	Description	Description	Pin Name	J1/J2 pin #
2	12P0V	+12V power	+3.3V power	3P3V	1

4	3P3V	3.3V power	+3.3V power	3P3V	3
6	GND	ground	Diff pair 24+/I2C CLK/SPI SCLK	D24_P/SCL/SCLK	5
8	CLK1_P	diff pair CLK1+	Diff pair 24- or SPI MOSI	D24_N/SDA/MOSI	7
10	CLK1_N	diff pair CLK1-	diff pair CLK0+	CLK0_P	9
12	B KEY	**key**	diff pair CLK0-	CLK0_N	11
14	B KEY	**key**	**key**	B KEY	13
16	B KEY	**key**	**key**	B KEY	15
18	B KEY	**key**	**key**	B KEY	17
20	GND	ground	**key**	B KEY	19
22	D12_P/CS	Diff pair 12+/SPI CS	Diff pair 0+	D0_P	21
24	D12_N/MISO	Diff pair 12-/SPI MISO	Diff pair 0-	D0_N	23
26	D13_P	Diff pair 13+	Diff pair 1+	D1_P	25
28	D13_N	Diff pair 13-	Diff pair 1-	D1_N	27
30	D14_P	Diff pair 14+	Diff pair 2+	D2_P	29
32	D14_N	Diff pair 14-	Diff pair 2-	D2_N	31
34	D15_P	Diff pair 15+	Diff pair 3+	D3_P	33
36	D15_N	Diff pair 15-	Diff pair 3-	D3_N	35
38	GND	ground	ground	GND	37
40	D16_P	Diff pair 16+	Diff pair 4+	D4_P	39
42	D16_N	Diff pair 16-	Diff pair 4-	D4_N	41
44	D17_P	Diff pair 17+	Diff pair 5+	D5_P	43
46	D17_N	Diff pair 17-	Diff pair 5-	D5_N	45
48	D18_P	Diff pair 18+	Diff pair 6+	D6_P	47
50	D18_N	Diff pair 18-	Diff pair 6-	D6_N	49
52	D19_P	Diff pair 19+	Diff pair 7+	D7_P	51
54	D19_N	Diff pair 19-	Diff pair 7-	D7_N	53
56	GND	ground	ground	GND	55
58	D20_P	Diff pair 20+	Diff pair 8+	D8_P	57
60	D20_N	Diff pair 20-	Diff pair 8-	D8_N	59
62	D21_P	Diff pair 21+	Diff pair 9+	D9_P	61
64	D21_N	Diff pair 21-	Diff pair 9-	D9_N	63
66	D22_P	Diff pair 22+	Diff pair 10+	D10_P	65
68	D22_N	Diff pair 22-	Diff pair 10-	D10_N	67
70	D23_P	Diff pair 23+	Diff pair 11+	D11_P	69
72	D23_N	Diff pair 23-	Diff pair 11-	D11_N	71
74	GND	ground	+5V power	5P0V	73
			+5V power	5P0V	75

Table 6 B-Keyed M.2 RF Module Connector pin-out

3.2. M.2 Clock Module Connector

The Clock Module connector is a 67-pin NGFF receptacle. The connector is a TE p/n 1-2199230-5 M-Keyed M.2 connector. The pin out is shown in Table 7.

J3 pin #	Pin Name	Description	Description	Pin Name	J3 pin #
2	12P0V	+12V power	+3.3V power	3P3V	1
4	3P3V	+3.3V power	+3.3V power	3P3V	3
6	GND	ground	Diff clock pair output 0+	CLK0_P	5
8	reserved		Diff clock pair output 0-	CLK0_N	7
10	reserved		ground	GND	9
12	reserved		Diff clock pair output 1+	CLK1_P	11
14	reserved		Diff clock pair output 1-	CLK1_N	13
16	reserved		ground	GND	15
18	reserved		Diff clock pair output 2+	CLK2_P	17
20	GND	ground	Diff clock pair output 2-	CLK2_N	19
22	reserved		ground	GND	21
24	reserved		Diff clock pair output 3+	CLK3_P	23
26	reserved		Diff clock pair output 3-	CLK3_N	25
28	reserved		ground	GND	27
30	reserved		GPS Freq/Phase input 0	FREQ_PHASE_0	29
32	reserved		ground	GND	31
34	reserved		GPS Freq/Phase input 1	FREQ_PHASE_1	33
36	reserved		ground	GND	35

38	GND	ground	GPS SPI select	GPS_SPI_CS	37
40	reserved		GPS SPI MISO	GPS_SPI_MISO	39
42	reserved		GPS SPI clock	GPS_SPI_SCLK	41
44	reserved		GPS SPI MOSI	GPS_SPI_MOSI	43
46	reserved		GPS I2C clock	GPS_I2C_SCL	45
48	reserved		GPS I2C data	GPS_I2C_SDA	47
50	reserved		ground	GND	49
52	reserved		GPS UART TXD	GPS_TXD	51
54	reserved		GPS UART RXD	GPS_RXD	53
56	GND	ground	ground	GND	55
58	GPS_REF_OUT	GPS reference clock output	GPS 1 PPS output	1PPS	57
60	M KEY	**key**	**key**	M KEY	59
62	M KEY	**key**	**key**	M KEY	61
64	M KEY	**key**	**key**	M KEY	63
66	M KEY	**key**	**key**	M KEY	65
68	REF_10M_IN	10MHz Reference input	ground	GND	67
70	GND	ground	GPS USB D-	GPS_D-	69
72	GPS_ANT	GPS antenna input	GPS USB D+	GPS_D+	71
74	GND	ground	+5V power	5P0V	73
			+5V power	5P0V	75

Table 7 M-Keyed M.2 Clock Module Connector pin-out

3.3. Clock and Timing Connectors

Clock Modules that contain a GPS module connect to SMA jacks on the DE. The functions are listed in the following three sections.

3.3.1. External Active GPS Antenna

This SMA jack is an RF Solutions p/n CON-SMA-EDGE-S. It is an RF input that connects to an active GPS antenna. The DE supplies power to this antenna. The power supply is current limited and short-proof.

3.3.2. External 10MHz Reference

This SMA jack is an RF Solutions p/n CON-SMA-EDGE-S. It is a digital input that accepts up to 5V signaling levels and can be used as a highly stable reference input to the Clock Module.

3.3.3. Clock Output

This SMA jack is an RF Solutions p/n CON-SMA-EDGE-S. It supplies a programmable frequency 3.3V digital clock output generated by the Clock Module that can be used as a highly stable clock source for external logic. It can be programmed to be synchronous with the FPGA and RF Module clocks for system expansion.

3.3.4. USB Micro-B GPSDO Clock Control Port

This USB port is routed to the Clock Module to allow programming of the on-board GPS, if fitted. It is an FCI p/n 10118192-0001LF USB 2.0 micro-B receptacle. The pin-out is shown in Table 8.

J7 pin #	GPSDO USB 2.0 Type B Pin Name	Description
1	Vbus	5V power
2	D-	data (-)
3	D+	data (+)
4	ID	Mode detect
5	GND	ground

Table 8 GPSDO USB 2.0 Port Connector Pin-out

3.4. FPGA and Support Connectors

3.4.1. Micro SDXC Socket

The micro-SDXC socket is a Molex p/n 0472192001 hinged type socket. See Table 9.

J8 pin #	Micro SDXC Pin Name	Description
1	DAT2	Data2
2	CD/DAT3	Data3
3	CMD	Command
4	3P3V	Power
5	CLK	Clock
6	GND	Power ground
7	DAT0	Data0
8	DAT1	Data1
9	GND	shield
10	GND	shield
11	GND	shield
12	GND	shield

Table 9 Micro-SDXC Socket Pin-out

3.4.2. FPGA JTAG Connector

The FPGA JTAG port is used to program the configuration SRAM and internal flash memory of the MAX10 FPGA, and to run the Signaltap logic analyzer.

The FPGA JTAG connector is a 10-pin, 2.54mm pitch vertical male pin header, 3M p/n 951210-8622-AR. See Table 10. It is designed to work with an Altera USB Blaster or equivalent.

J9 pin #	JTAG Header Pin Name	Description
1	TCK	JTAG TCK
2	GND	ground
3	TDO	JTAG TDO
4	+3.3V	Target power supply
5	TMS	JTAG TMS
6	n/c	
7	n/c	
8	n/c	
9	TDI	JTAG TDI
10	GND	ground

Table 10 S7 MCU JTAG connector pin-out

3.5. Communications Connectors

3.5.1. Gigabit Ethernet Connectors

The DE Ethernet connectors are Bel Fuse L836-1J1T-43 right-angle RJ-45 MagJacks. The pin outs are shown in Table 11 and Table 12.

J10 pin #	Ethernet 1 Pin Name	Description
1	ETH1_TD+	transmit data (+)
2	ETH1_TD-	transmit data (-)
3	ETH1_RD+	receive data (+)
4	ETH1_CTD	transmit data CT
5	ETH1_CRD	receive data CT
6	ETH1_RD-	receive data (-)
7		not used
8	ETH1_shield	shield
9	ETH1_LF_GK_YA	Left side: Green LED cathode, yellow LED anode
10	ETH1_LF_GA_YK	Left side: Green LED anode, yellow LED cathode
11	ETH1_RT_GA_YK	Right side: Green LED anode, yellow LED cathode
12	ETH1_RT_GK_YA	Right side: Green LED cathode, yellow LED anode

Table 11 Ethernet Port 1 Connector Pin-out

J11 pin #	Ethernet 2 Pin Name	Description
1	ETH2_TD+	transmit data (+)
2	ETH2_TD-	transmit data (-)
3	ETH2_RD+	receive data (+)
4	ETH2_CTD	transmit data CT
5	ETH2_CRD	receive data CT
6	ETH2_RD-	receive data (-)
7		not used
8	ETH2_shield	shield
9	ETH2_LF_GK_YA	Left side: Green LED cathode, yellow LED anode
10	ETH2_LF_GA_YK	Left side: Green LED anode, yellow LED cathode
11	ETH2_RT_GA_YK	Right side: Green LED anode, yellow LED cathode
12	ETH2_RT_GK_YA	Right side: Green LED cathode, yellow LED anode

Table 12 Ethernet port 2 Connector Pin-out

3.5.2. USB Connectors

There are two USB connectors on the Data Engine. The USB 2.0 host port is a type-A receptacle. The USB 3.0 peripheral port is a microUSB type B receptacle.

3.5.2.1. High-Speed USB 2.0 Host Port

The USB 2.0 host port connector is a right-angle type A receptacle, Amphenol p/n UE27AC54100. See Table 13.

J12 pin #	USB 2.0 Type A Pin Name	Description

1	Vbus	5V power
2	D-	data (-)
3	D+	data (+)
4	GND	n/c

Table 13 USB 2.0 Host Port Connector Pin-out

3.5.2.2. SuperSpeed USB 3.0 Peripheral Port

The SuperSpeed USB 3.0 peripheral port connector is a right-angle USB 3.0 micro-B receptacle, Amphenol p/n GSB3433K33HR. See Table 14.

J13 pin #	USB 3.0 Micro-B Pin Name	Description
1	Vbus	5V power
2	D-	USB 2.0 data (-)
3	D+	USB 2.0 data (+)
4	OTG_ID	USB OTG ID
5	GND	power ground
6	SSTX-	USB 3.0 signal transmit (-)
7	SSTX+	USB 3.0 signal transmit (+)
8	GND	power ground
9	SSRX-	USB 3.0 signal receive (-)
10	SSRX+	USB 3.0 signal receive (+)

Table 14 GPS configuration USB connector pin out

3.5.1. WiFi Antenna Connector

The WiFi module connects to an optional external antenna via a U.FL connector, Hirose part number U.FL-R-SMT(10).

3.6. Expansion Connectors

Expansion connectors are provided for connection an SBC, SBC hat, Arduino shield, mikroBUS™ Click™ module, Ultra96 mezzanine board, Pmod™ boards and Grove sensor boards. Two analog I/O headers are provided, as well as a non-specific GPIO header for connection to custom low-speed TangerineSDR expansion shields.

3.6.1. SBC Hat/Host Connector

The SBC Hat/Host expansion connector is a 40-pin, dual row (2x20) 0.100” pitch, long-pin header, Adafruit p/n 2223 (Mouser p/n 485-2223) , with the female sockets mounted on the bottom of the board with the pins sticking out the top of the board. The DE may be directly plugged into a Raspberry Pi 3B+ or an Odroid N2 SBC, while RPi compatible hats may be plugged directly onto the DE top connector pins. The pin-out is in Table 15.

J15/P1 pin #	RPi 3B Pin Name	ODRIOD N2 Pin Name	ODROID N2 Pin Name	RPi 3B Pin Name	J15/P1 pin #
1	3.3V	3.3V	5.0V	5.0V	2
3	BCM2/SDA	I2C-2 SDA/GPIOX.17	5.0V	5.0V	4
5	BCM3/SCL	I2C-2 SCL/GPIOX.18	GND	GND	6
7	BCM4/GPCLK0	GPIOA.13	TXD1/GPIOX.12	BCM14/TXD	8
9	GND	GND	RXD1/GPIOX.13	BCM15/RXD	10

11	BCM17	GPIOX.3	PWM_E/GPIOX.16	BCM18/PWM0	12
13	BCM27	GPIOX.4	GND	GND	14
15	BCM22	GPIOX.7		BCM23	16
17	3.3V	3.3V		BCM24	18
19	BCM10/MOSI	SPIo_MOSI/GPIOX.8		GND	20
21	BCM9/MISO	SPIo_MISO/GPIOX.9		BCM25	22
23	BCM11/SCLK	SPIo_CLK/GPIOX.11		BCM8/CE0	24
25	GND	GND		BCM7/CE1	26
27	BCM0/ID_SD	I2C-3 SDA/GPIOA.14		BCM1/ID_SC	28
29	BCM5	GPIOX.14	GND	GND	30
31	BCM6	GPIOX.15		BCM12/PWM0	32
33	BCM13/PWM1	GPIOX.5	GND	GND	34
35	BCM19/MISO	GPIOX.6		BCM16	36
37	BCM26	ADC.AIN3	REF 1.8V	BCM20/MOSI	38
39	GND	GND	ADC.AIN2	BCM21/SCLK	40

Table 15 SBC Hat/Host Connector Pin-out

3.6.2. Arduino Shield Connectors

The Arduino R3 shield mounts to the DE on five connectors. Four single-row connectors: one 6-pin, two 8-pin and one 10-pin, arranged in two parallel rows, with the 8-pin and 6-pin on one side and the other 8-pin and the 10-pin on the other side. A 6-pin dual-row connector mounts perpendicularly between the two rows at the bottom, for a total of 38 interface pins. See Table 16 through Table 20 for connections.

The connectors may be long-tail female connectors, allowing shields to be stacked above or below the DE, but the standard connectors are short-tail female connectors, allowing shields to be stacked only above the DE. The connectors are Amphenol/FCI p/n 66951-006LF (6-pin single row), 66951-008LF (8-pin single row), 66951-010LF (10-pin single row) and 66953-003LF (6-pin dual-row).

J16 pin #	Upper Left Arduino Connector Pin Name	Description
1	n/c	No connection
2	IOREF	
3	Reset	
4	3.3V	3.3V power
5	5.0V	5.0V power
6	GND	ground
7	GND	ground
8	Vin	

Table 16 Upper Left (8 pin) Arduino Connector Pin-out

J17 pin #	Lower Left Arduino Connector Pin Name	Description
1	A0	Analog input 0
2	A1	Analog input 1
3	A2	Analog input 2
4	A3	Analog input 3
5	A4/SDA	Analog input 4/I2C Data
6	A5/SCL	Analog input 5/I2C Clock

Table 17 Lower Left (6 pin) Arduino Connector Pin-out

J18 pin #	Upper Left Arduino Connector Pin Name	Description
1	D7	Digital I/O7
2	D6/PWM6	Digital I/O6/PWM
3	D5/PWM5	Digital I/O5/PWM

4	D4	Digital I/O4
5	D3/PWM3/INT1	Digital I/O3/PWM/Interrupt
6	D2/INT0	Digital I/O2/Interrupt
7	D1/TXD	Digital I/O1/UART TXD
8	D0/RXD	Digital I/O0/UART TXD

Table 18 Lower Right (8 pin) Arduino Connector Pin-out

J19 pin #	Upper Left Arduino Connector Pin Name	Description
1	GPIO18/ADC4/SCL	I2C Clock
2	GPIO17/ADC5/SDA	I2C Data
3	AREF	
4	GND	ground
5	D13/SCK	Digital I/O13/SPI Clock
6	D12/MISO	Digital I/O12/SPI MISO
7	D11/MOSI/PWM11	Digital I/O11/SPI MOSI/PWM
8	D10/CS/PWM10	Digital I/O10/SPI CS/PWM
9	D9/PWM9	Digital I/O9/PWM
10	D8	Digital I/O8

Table 19 Upper Right (10 pin) Arduino Connector Pin-out

J20 pin #	Upper Left Arduino Connector Pin Name	Description
1	MISO	SPI MISO
2	5.0V	5.0V power
3	SCK	SPI Clock
4	MOSI	SPI MOSI
5	Reset	
6	GND	ground

Table 20 Center Dual-Row (6 pin) Arduino Connector Pin-out

3.6.3. mikroBUS™ (Click™) Connectors

The mikroBUS™ Click board™ uses two 8-pin, single row, 0.100” pitch receptacles, TE p/n 215297-8. The connectors are individually numbered and simply referred to as “left” (see Table 21) and “right” (see Table 22); the right-hand one is marked on the silk screen with a diagonal line below pin 8.

J21 pin #	mikroBUS™ Left Connector Pin Name	Description
1	AN/RA2	Analog in
2	RST/RE1	Reset
3	CS/RE0	SPI CS
4	SCK/RC3	SPI Clock
5	MISO/RC4	SPI MISO
6	MOSI/RC5	SPI MOSI
7	3.3V	3.3V power
8	GND	ground

Table 21 mikroBUS™ Left Connector Pin-out

J22 pin #	mikroBUS™ Right Connector Pin Name	Description
1	RC0/PWM	PWM
2	RB0/INT	Interrupt
3	RC7/RX	UART TXD
4	RC6/TX	UART RXD
5	RC3/SCL	I2C Clock
6	RC4/SDA	I2C Data
7	+5.0V	+5V power
8	GND	ground

Table 22 mikroBUS™ Right Connector Pin-out

3.6.4. Ultra96 Mezzanine Connectors

The Ultra96 mezzanine board uses two connectors, one for low-speed I/O and power and the other for high-speed I/O only. Some mezzanine boards may use only the low-speed connector.

The Ultra96 low-speed I/O connector is a 40-pin, 2.0mm pitch, dual row female header, Amphenol p/n 55510-140LF. It contains 32 signals. The pin-out is shown in Table 23.

J23 pin #	Pin Name	Description	Description	Pin Name	J23 pin #
1	GND	ground	ground	GND	2
3	HD_GPIO_0			POWER_PB_B	4
5	HD_GPIO_1			PS_POR_PB_B	6
7	HD_GPIO_2			MIO38_SPI0_SCLK	8
9	HD_GPIO_3			MIO42_SPI0_MISO	10
11	HD_GPIO_4			MIO41_SPI0_CS	12
13	HD_GPIO_5			MIO43_SPI0_MOSI	14
15	LSEXP_I2C0_SCL			HD_GPIO_9	16
17	LSEXP_I2C0_SDA			HD_GPIO_10	18
19	LSEXP_I2C1_SCL			HD_GPIO_11	20
21	LSEXP_I2C1_SDA			HD_GPIO_12	22
23	MIO36_PS_GPIO1_0			MIO37_PS_GPIO1_1	24
25	MIO39_PS_GPIO1_2			MIO40_PS_GPIO1_3	26
27	MIO44_PS_GPIO1_4			MIO45_PS_GPIO1_5	28
29	HD_GPIO_6			HD_GPIO_13	30
31	HD_GPIO_7			HD_GPIO_14	32
33	HD_GPIO_8			HD_GPIO_15	34
35	VCC_PSAUX			VSYS_IN	36
37	VCC_5V0			VSYS_IN	38
39	GND	ground	ground	GND	40

Table 23 Ultra96 Low-speed I/O Connector Pin-out

The Ultra96 high-speed I/O connector is a 60-pin, 0.8mm pitch dual-row receptacle, FCI p/n 61082-061409LF. The pin-out is shown in Table 24.

J24 pin #	Pin Name	Description	Description	Pin Name	J24 pin #
1	MIO11_SPI1_MOSI			CSI0_C_P	2
3	n/c			CSI0_C_N	4
5	n/c		ground	GND	6
7	MIO9_SPI1_CS			CSI0_D0_P	8
9	MIO6_SPI1_SCLK			CSI0_D0_N	10
11	MIO10_SPI1_MISO		ground	GND	12
13	GND	ground		CSI0_D1_P	14
15	CSI0_MCLK			CSI0_D1_N	16
17	CSI1_MCLK		ground	GND	18
19	GND	ground		CSI0_D2_P	20
21	DSI_CLK_P			CSI0_D2_N	22
23	DSI_CLK_N		ground	GND	24
25	GND	ground		CSI0_D3_P	26
27	DSI_D0_P			CSI0_D3_N	28
29	DSI_D0_N		ground	GND	30
31	GND	ground		HSEXP_I2C2_SCL	32
33	DSI_D1_P			HSEXP_I2C2_SDA	34
35	DSI_D1_N			HSEXP_I2C3_SCL	36
37	GND	ground		HSEXP_I2C3_SDA	38
39	DSI_D2_P		ground	GND	40

41	DSI_D2_N			CSI1_D0_P	42
43	GND	ground		CSI1_D0_N	44
45	DSI_D3_P		ground	GND	46
47	DSI_D3_N			CSI1_D1_P	48
49	GND	ground		CSI1_D1_N	50
51	USB2D3_P		ground	GND	52
53	USB2D3_N			CSI1_C_P	54
55	GND	ground		CSI1_C_N	56
57	HSIC_STR		ground	GND	58
59	HSIC_DATA		Pullup to VCC_PSAUX	PULLUP	60

Table 24 Ultra96 High-speed I/O Connector Pin-out

3.6.5. Pmod™ Port Connectors

The Pmod™ connectors are each 12-pin 2.54mm right-angle female receptacles, Samtec part number SSQ-106-02-T-D-RA. See Table 25 and Table 26. Note that Pmod™ connectors are numbered differently than standard rectangular headers (down one side, then down the other, placing pins 1 and 7 in adjacent rows). Also note that pins 1-4 and 7-10 are FPGA programmable pins, so they may be assigned any GPIO function.

J25 pin #	Pmod1 Connector Pin Name	Description
1	IO1/CS/CTS/DIR/DIR1/NC/LRCLK	GPIO/SPI/UART/H-BR/Dual H-BR/Exp Dual H-BR/I2C/I2S
2	IO2/MOSI/TXD/EN/EN1/NC/DAC Data	GPIO/SPI/UART/H-BR/Dual H-BR/Exp Dual H-BR/I2C/I2S
3	IO3/MISO/RXD/SA/DIR2/SCL/ADC Data	GPIO/SPI/UART/H-BR/Dual H-BR/Exp Dual H-BR/I2C/I2S
4	IO4/SCK/RTS/SB/EN2/SDA/BCLK	GPIO/SPI/UART/H-BR/Dual H-BR/Exp Dual H-BR/I2C/I2S
5	GND	ground
6	VCC	3.3V or 5.0V
7	IO5/DIR2	GPIO/Exp Dual H-BR
8	IO6/EN2	GPIO/Exp Dual H-BR
9	IO7/S2A	GPIO/Exp Dual H-BR
10	IO8/S2B	GPIO/Exp Dual H-BR
11	GND	ground
12	VCC	3.3V or 5V

Table 25 Pmod1 Connector Pin-out

J26 pin #	Pmod1 Connector Pin Name	Description
1	IO1/CS/CTS/DIR/DIR1/NC/LRCLK	GPIO/SPI/UART/H-BR/Dual H-BR/Exp Dual H-BR/I2C/I2S
2	IO2/MOSI/TXD/EN/EN1/NC/DAC Data	GPIO/SPI/UART/H-BR/Dual H-BR/Exp Dual H-BR/I2C/I2S
3	IO3/MISO/RXD/SA/DIR2/SCL/ADC Data	GPIO/SPI/UART/H-BR/Dual H-BR/Exp Dual H-BR/I2C/I2S
4	IO4/SCK/RTS/SB/EN2/SDA/BCLK	GPIO/SPI/UART/H-BR/Dual H-BR/Exp Dual H-BR/I2C/I2S
5	GND	ground
6	VCC	3.3V or 5.0V
7	IO5/DIR2	GPIO/Exp Dual H-BR
8	IO6/EN2	GPIO/Exp Dual H-BR
9	IO7/S2A	GPIO/Exp Dual H-BR
10	IO8/S2B	GPIO/Exp Dual H-BR
11	GND	ground
12	VCC	3.3V or 5V

Table 26 Pmod2 Connector Pin-out

3.6.6. Grove Connectors

Two Grove connectors are provided, one with an analog pin-out and one with a digital pin-out.

3.6.6.1. Grove Analog Connector

The Grove analog connector is a 4-pin, shrouded vertical pin-type connector, Seeed p/n 110990030. The two signal pins are 3.3V analog inputs. See Table 27

J27 pin #	Grove Analog Connector Pin Name	Description
1	AIN0	Analog input
2	AIN1	Analog input
3	+3.3V	3.3V power
4	GND	ground

Table 27 Grove Analog Connector Pin-out

3.6.6.2. Grove Digital Connector

The Grove Digital connector is a 4-pin, shrouded vertical pin-type connector, Seeed p/n 110990030. The two digital pins are programmable, allowing I2C, UART or GPIO connections. See Table 28.

J28 pin #	Grove Digital Connector Pin Name	Description
1	SCL, RXD, D0	I2C clock, UART RXD, GPIO pin
2	SDA, TXD, D1	I2C data, UART TXD, GPIO pin
3	+3.3V	3.3V power
4	GND	ground

Table 28 Grove Digital Connector Pin-out

3.6.7. Low-speed Digital GPIO Connector

The low-speed I/O connector consists of a 40-pin, dual-row, 0.100” header, Amphenol p/n 68602-440HLF. The pin-out is shown in Table 29.

J29 pin #	Pin Name	Description	Description	Pin Name	Jxx pin #
1	GND	ground	Digital I/O pin 0	DIO0	2
3	GND	ground	Digital I/O pin 1	DIO1	4
5	GND	ground	Digital I/O pin 2	DIO2	6
7	GND	ground	Digital I/O pin 3	DIO3	8
9	GND	ground	Digital I/O pin 4	DIO4	10
11	GND	ground	Digital I/O pin 5	DIO5	12
13	GND	ground	Digital I/O pin 6	DIO6	14
15	GND	ground	Digital I/O pin 7	DIO7	16
17	GND	ground	Digital I/O pin 8	DIO8	18
19	GND	ground	Digital I/O pin 9	DIO9	20
21	GND	ground	Digital I/O pin 10	DIO10	22
23	GND	ground	Digital I/O pin 11	DIO11	24
25	GND	ground	Digital I/O pin 12	DIO12	26
27	GND	ground	Digital I/O pin 13	DIO13	28
29	GND	ground	Digital I/O pin 14	DIO14	30
31	GND	ground	Digital I/O pin 15	DIO15	32
33	GND	ground	Digital I/O pin 16	DIO16	34
35	GND	ground	Digital I/O pin 17	DIO17	36
37	GND	ground	Digital I/O pin 18	DIO18	38
39	GND	ground	Digital I/O pin 19	DIO19	40

Table 29 Low-speed Digital GPIO Connector Pin-out

3.6.8. Analog I/O Connectors

Each analog I/O connector is a 10-pin, 2.54mm pitch vertical male header, 3M p/n 951210-8622-AR. The pin-out of the analog input connector is shown in Table 30, and the analog output connector is shown in Table 31.

J30 pin #	Analog In Connector Pin Name	Description
1	GND	ground
2	AIN0	Analog input 0
3	GND	ground
4	AIN1	Analog input 0
5	GND	ground
6	AIN2	Analog input 0
7	GND	ground
8	AIN3	Analog input 0
9	GND	ground
10	3P3V	+3.3V power

Table 30 Analog Input Connector Pin-out

J31 pin #	Analog Out Connector Pin Name	Description
1	GND	ground
2	AOUT0	Analog output 0
3	GND	ground
4	AOUT1	Analog output 0
5	GND	ground
6	AOUT2	Analog output 0
7	GND	ground
8	AOUT3	Analog output 0
9	GND	ground
10	3P3V	+3.3V power

Table 31 Analog Output Connector Pin-out

3.7. Power Input Connector

The external 12V power supply connector is a 5.5mm O.D., 2.1mm pin, right-angle coaxial receptacle, Tensility p/n 54-00127, (see Table 32). All power is supplied to the DE via this connector.

J32 pin #	Power Connector Pin Name	Description
pin	+12VDC	Nominal +12VDC power input to DE
shield	GND	GND

Table 32 External Power Supply Connector

3.8. System Resources and I/O

3.8.1. Jumpers

The DE implements 8 jumpers. Four are for configuration and four are for spares. They are listed in Table 33 and Table 34.The spare jumpers are included for possible future use. The 4-position jumpers are made from 2mm headers, 3M p/n 951208-8622-AR

(alternate Harwin p/n M22-2520405). Mating parts are 2mm shorting jumpers with finger grip, Sullins p/n NPN02SXLN-RC (alternate without grip, Samtec p/n 2SN-BK-G). Configuration jumpers have optional pull-down resistors to eliminate the need for jumpers for manufactured variants.

Config Header pins	Silkscreen Label	Description
1-2	***TBD***	***TBD***
3-4	***TBD***	***TBD***
5-6	***TBD***	***TBD***
7-8	***TBD***	***TBD***

Table 33 Configuration Jumpers

Spare Header pins	Silkscreen Label	Description
1-2	***TBD***	***TBD***
3-4	***TBD***	***TBD***
5-6	***TBD***	***TBD***
7-8	***TBD***	***TBD***

Table 34 Spare Jumpers

3.8.2. Fan Power Connector

The fan power connector is a 2-pin, 2.54mm pitch, vertical male header, Molex p/n 0901310121, (see Table 35). Fan power is supplied by the DE to an off-board fan via this connector.

J33 pin #	Fan Power Connector Pin Name	Description
1	+5V_FAN	+5VDC switched fan power
2	GND	GND

Table 35 Fan Power Connector

3.8.3. Buffered I/O

3.8.3.1. PTT/Keyer Paddle Input Connector

The PTT and Keyer paddle input connector is a 4 conductor, 3.5mm jack, CUI p/n SJ-43515TS. The pin-out is shown in Table 36.

J34 pin #	PTT/Keyer Connector Pin Name	Description
1 (tip)	dot	Paddle dot or straight key contact
2 (ring 1)	dash	Paddle dash contact
3 (ring 2)	PTT	Microphone push to talk contact
4 (sleeve)	GND	ground

Table 36 PTT/Keyer Paddle Input Connector

3.8.3.2. Buffered Amplifier Keying Output Connector

The amplifier keying output connector is a 2 conductor, 3.5mm jack, CUI p/n SJ2-35852B-SMT-TR. The pin-out is shown in Table 37.

J35 pin #	Amp Key Connector Pin Name	Description
1 (tip)	amp_key	Amplifier keying output (active low)
2 (sleeve)	GND	ground

Table 37 Amplifier Key Output Connector

3.8.4. Spare I/O Pins

Spare FPGA I/O pins may be routed to one or more header connectors or test points. These headers will not be installed on the PCB (they will be listed as “DNI” or “Do Not Install” in the BOM). Pin outs and appropriate connector part numbers will be listed as connectors are added.

3.8.5. Test Points

Test points will be provided as required to allow for manufacturing test. Test points will not be added to nets that already contain one or more through-hole part pins.

4. Data Engine FPGA Pinout

The FPGA pins and banks are mapped to functions as shown in Table 38 through Table 46.

FPGA Bank	FPGA pin name	Pin #	Function

Table 38 FPGA Bank and Pin Assignments

FPGA pin	Package pin	I/O dir	I/O type	I/O level

Table 39 Bank 1 pin functions

FPGA pin	Package pin	I/O dir	I/O type	I/O level

Table 40 Bank 2 pin functions

FPGA pin	Package pin	I/O dir	I/O type	I/O level

Table 41 Bank 3 pin functions

FPGA pin	Package pin	I/O dir	I/O type	I/O level

Table 42 Bank 4 pin functions

FPGA pin	Package pin	I/O dir	I/O type	I/O level

Table 43 Bank 5 pin functions

FPGA pin	Package pin	I/O dir	I/O type	I/O level

Table 44 Bank 6 pin functions

FPGA pin	Package pin	I/O dir	I/O type	I/O level

Table 45 Bank 7 pin functions

FPGA pin	Package pin	I/O dir	I/O type	I/O level

Table 46 Bank 8 pin functions